18V, Ultra-Low 2uA IQ，Low Noise LDO Regulators

FEATURES

- Low Dropout Voltage：160mV@100mA
- Low Quiescent Current：2μA(typ.)
- High Ripple Rejection：65dB@1kHz
- Operating Voltage Range：2.5V～18V
- Output Voltage Range：1.2V ~ 5.0V
- High Accuracy：±2%（Typ.）
- Low Output Noise: 27xV_{OUT} μV_{RMS} (10Hz~100kHz)
- 300mA Output Current
- Built-in Current Limiter, Thermal shutdown and Short-Circuit Protection
- Available in Green SOT89-3 、SOT23-3 、DFN1*1-4 AND SOT23-5 Packages

DESCRIPTIONS

The DP31311 series are a group of positive voltage regulators manufactured by CMOS technologies with low power consumption and low dropout voltage, which provide large output currents even when the difference of the input-output voltage is small.

The DP31311 series can deliver 300mA output current and allow an input voltage as high as 18V. The series are very suitable for the battery-powered equipments, such as RF applications and other systems requiring a quiet voltage source.

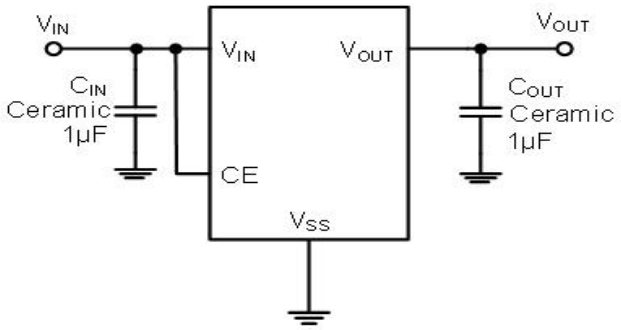
APPLICATIONS

- Cordless Phones
- Radio control systems
- Laptop, Palmtops and PDAs
- Single-lens reflex DSC
- PC peripherals with memory
- Wireless Communication Equipments
- Portable Audio Video Equipments
- Car Navigation Systems
- LAN Cards
- Ultra Low Power Microcontroller

ORDERING INFORMATION

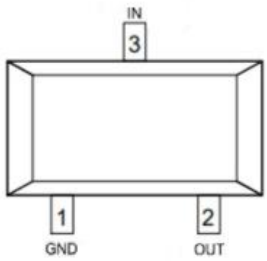
Part Number	Description
SOT23-3	Pb free in T&R, 3000 Pcs/Reel
XTDFN-1×1-4L	Pb free in T&R, 10000 Pcs/Reel
SOT89-3	Pb free in T&R, 1000 Pcs/Reel
SOT23-5	Pb free in T&R, 3000 Pcs/Reel

TYPICAL APPLICATION CIRCUIT

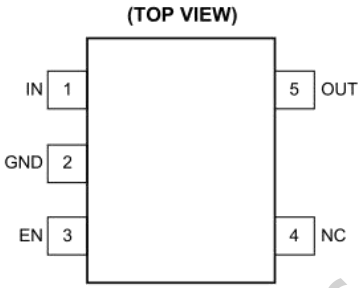


PRODUCT DESCRIPTION

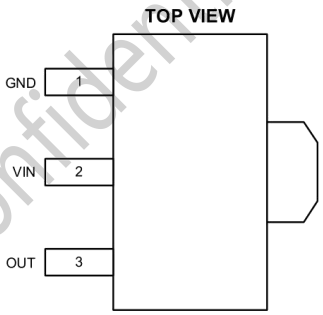
➢ Pin Arrangement



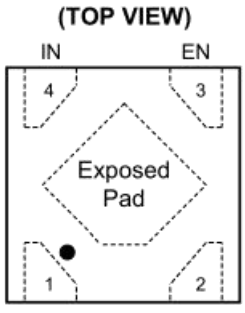
SOT-23-3



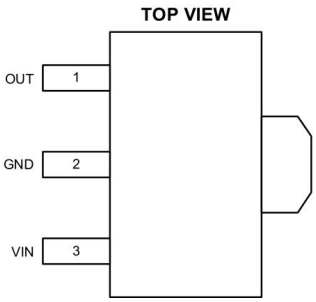
SOT-23-5



SOT89-3A



XTDFN-1×1-4L

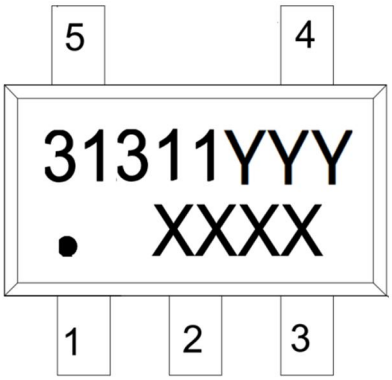


SOT89-3B

➢ Pin Configuration

SOT23-3	SOT89-3A	SOT23-5	SOT89-3B	DFN1*1-4	Pin Name	Description
1	1	2	2	2	GND	Ground.
2	2	1	3	4	VIN	Input Supply of the LDO.
3	3	5	1	1	OUT	Regulator Output Pin. It is recommended to use a ceramic capacitor with effective capacitance in the range of 1μF to 10μF to ensure stability. This ceramic capacitor should be placed as close as possible to OUT pin.
-	-	3	-	3	EN	Enable Pin. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. This pin must be pulled high by an external resistor connected to IN pin if EN pin is not used.
-	-	4	-	-	NC	No Connection.
-	-	-	-	Exposed Pad	GND	Exposed Pad. Connect it to a large ground plane to maximize thermal performance.

➢ Marking Information



DP31311 for product name:

YYY refers to the following table description, represents different packaging and special output voltage

XXXX The first X represents the last year,2020 is 0;The second X represents the month,inA-L 12 letters;The third and fourth X on behalf of the date,01-31said;

Marking	Model	VOUT Voltage	PACKAGE
11-12	DP31311-12AST	1.2V	SOT23-3
11-15	DP31311-15AST	1.5V	SOT23-3
11-18	DP31311-18AST	1.8V	SOT23-3
11-25	DP31311-25AST	2.5V	SOT23-3
11-28	DP31311-28AST	2.8V	SOT23-3
11-30	DP31311-30AST	3.0V	SOT23-3
11-33	DP31311-33AST	3.3V	SOT23-3
11-38	DP31311-38AST	3.8V	SOT23-3
11-42	DP31311-42AST	4.2V	SOT23-3
11-50	DP31311-50AST	5.0V	SOT23-3

11A-12	DP31311-12BST	1.2V	SOT89-3A
11A-15	DP31311-15BST	1.5V	SOT89-3A
11A-18	DP31311-18BST	1.8V	SOT89-3A
11A-25	DP31311-25BST	2.5V	SOT89-3A
11A-28	DP31311-28BST	2.8V	SOT89-3A
11A-30	DP31311-30BST	3.0V	SOT89-3A
11A-33	DP31311-33BST	3.3V	SOT89-3A
11A-38	DP31311-38BST	3.8V	SOT89-3A
11A-42	DP31311-42BST	4.2V	SOT89-3A
11A-50	DP31311-50BST	5.0V	SOT89-3A
11B-12	DP31311-12CST	1.2V	SOT89-3B
11B-15	DP31311-15CST	1.5V	SOT89-3B
11B-18	DP31311-18CST	1.8V	SOT89-3B
11B-25	DP31311-25CST	2.5V	SOT89-3B
11B-28	DP31311-28CST	2.8V	SOT89-3B
11B-30	DP31311-30CST	3.0V	SOT89-3B
11B-33	DP31311-33CST	3.3V	SOT89-3B
11B-38	DP31311-38CST	3.8V	SOT89-3B
11B-42	DP31311-42CST	4.2V	SOT89-3B
11B-50	DP31311-50CST	5.0V	SOT89-3B

31311-12	DP31311-12DST	1.2V	SOT23-5
31311-15	DP31311-15DST	1.5V	SOT23-5
31311-18	DP31311-18DST	1.8V	SOT23-5
31311-25	DP31311-25DST	2.5V	SOT23-5
31311-28	DP31311-28DST	2.8V	SOT23-5
31311-30	DP31311-30DST	3.0V	SOT23-5
31311-33	DP31311-33DST	3.3V	SOT23-5
31311-38	DP31311-38DST	3.8V	SOT23-5
31311-42	DP31311-42DST	4.2V	SOT23-5
31311-50	DP31311-50DST	5.0V	SOT23-5
31311-12	DP31311-12ETD	1.2V	XTDFN-1×1-4L
31311-15	DP31311-15ETD	1.5V	XTDFN-1×1-4L
31311-18	DP31311-18ETD	1.8V	XTDFN-1×1-4L
31311-25	DP31311-25ETD	2.5V	XTDFN-1×1-4L
31311-28	DP31311-28ETD	2.8V	XTDFN-1×1-4L
31311-30	DP31311-30ETD	3.0V	XTDFN-1×1-4L
31311-33	DP31311-33ETD	3.3V	XTDFN-1×1-4L
31311-38	DP31311-38ETD	3.8V	XTDFN-1×1-4L
31311-42	DP31311-42ETD	4.2V	XTDFN-1×1-4L
31311-50	DP31311-50ETD	5.0V	XTDFN-1×1-4L

➢ Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)(1)

PARAMETER		Min	Max	Unit
VIN Voltage(1)		-0.3	24	V
EN Voltage		-0.3	24	V
VOUT Voltage(2)		-0.3	10	V
Output Current		-	400	mA
Power Dissipation	SOT23-5	-	600	mW
	SOT89-3A	-	800	mW
	SOT89-3B	-	800	mW
	XTDFN-1×1-4L	-	250	mW
	SOT23-3	-	500	mW
Operating free air temperature range		-40	85	℃
Operating junction temperature,TJ		-40	150	℃
Storage temperature, Tstg		-65	150	℃
Lead Temperature（Soldering，10sec.)		-	260	℃

Note:(1)Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute – maximum – rated conditions for extended periods may affect device reliability.

（2）All voltage values are with respect to network ground terminal

➢ Recommended Operating Conditions

PARAMETER	Min	Max	Unit
VIN Voltage(V_{IN})	2.5	18	V
VOUT Voltage(V_{OUT})	1.2	5	V
Output current(I_{OUT})	-	300	mA
TJ	-40	125	℃

Note : (1)All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using

standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

➢ ESD Ratings

PARAMETER	Description	Value	Unit
HBM	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
CDM	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	V

Note : (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

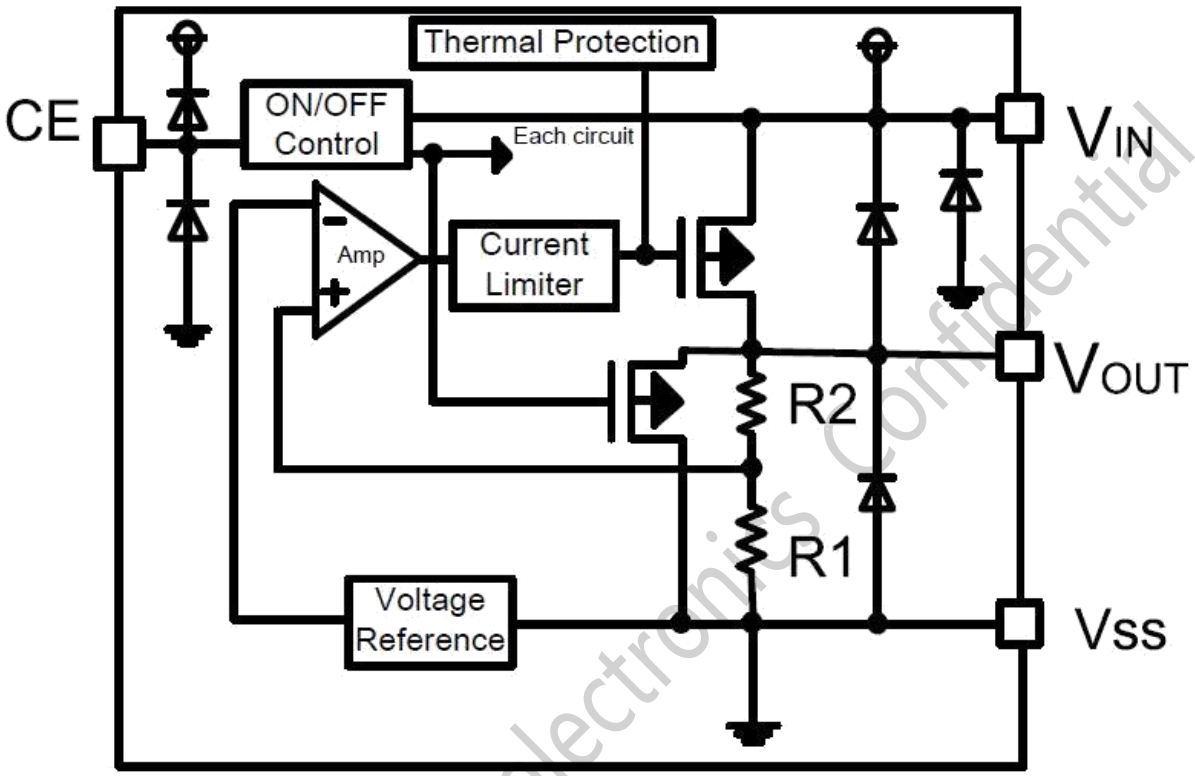
➢ Thermal Information

THERMAL METRIC	Description	SOT23-5	SOT89-3A	SOT89-3B	XTDFN-1×1-4L	SOT23-3	Unit
$R_{\theta JA}$	Junction-to-ambient thermal	191.6	55	55	166.1	208	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal	141.4	88	88	103.6	112	℃/W
$R_{\theta JB}$	Junction-to-board(Bottom)	44.5	9.6	9.6	110.6	56	℃/W
ψ_{JT}	Junction-to-top characterization	34.5	6.2	6.2	3.0	9.2	℃/W
ψ_{JB}	Junction-to-board	43.9	9.7	9.7	103.3	52	℃/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

BLOCK DIAGRAM



Future 1 Functional Block Diagram

ELECTRICAL CHARACTERISTICS

V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF，T_A=25℃,unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}	-	2.5	-	18	V
Output Voltage	V_{OUT}	I_{OUT}=1mA	VOUT* 0.98	-	VOUT* 1.02	V
Supply Current	I_Q	I_{OUT}=0mA		2		uA
Standby Current	I_{SHDN}	V_{EN}=0V		0.2	1	uA
Output Current	I_{OUT}	-		300		mA
Dropout Voltage	V_{DROP}	Iout=60mA Vout=5V		60		mV
		Iout=100mA Vout=5V		150		mV
		Iout=200mA Vout=5V		250		mV
		Iout=300mA Vout=5V		400		mV
Load Regulation	ΔV_{OUT}	V_{IN}= V_{OUT} +1V, 1mA≤I_{OUT}≤100mA		10		mV
Line Regulation	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$	I_{OUT} =10mA V_{OUT} +1V≤V_{IN}≤18V		0.01	0.2	%/V
Output Voltage Temperature Characteristics	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta T_A}$	I_{OUT} =10mA -40≤T≤+85℃		50		ppm
Output Current Limit	I_{LIM}	V_{OUT}= 0.5 x $V_{OUT(Normal)}$, V_{IN} = 5V		350		mA
Short Current	Ishort	V_{OUT}=0V		100		mA
Power Supply Rejection Rate	PSRR	F=100HZ Iout=50mA		80		dB
		F=1KHZ Iout=50mA		65		
		F=10KHZ Iout=50mA		50		
		F=100KHZ Iout=50mA		45		
EN Rising Threshold	$V_{EN(R)}$		1.5			V
EN Falling Threshold	$V_{EN(F)}$				0.3	V
Over-Temperature Protection	T_{SD}			160		℃
Over-Temperature Protection hysteresis	△T_{SD}			20		℃
COUT Auto-Discharge Resistance	$R_{DISCHRG}$	V_{IN}=5V, V_{OUT}=3.0V, V_{CE}=V_{SS}		150		Ω

TYPICAL CHARACTERISTICS

TJ = +25℃, VIN = (VOUT(NOM) + 1V) (whichever is greater), VEN = VIN, CIN = COUT = 1μF, unless otherwise noted.

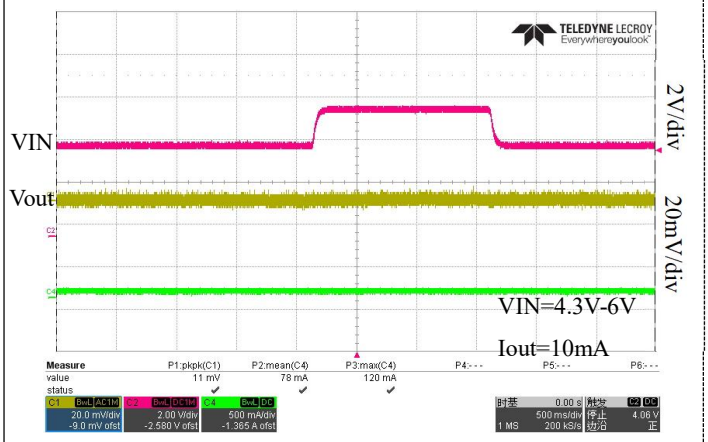


Figure1 Vout=3.3V Line Transient Response

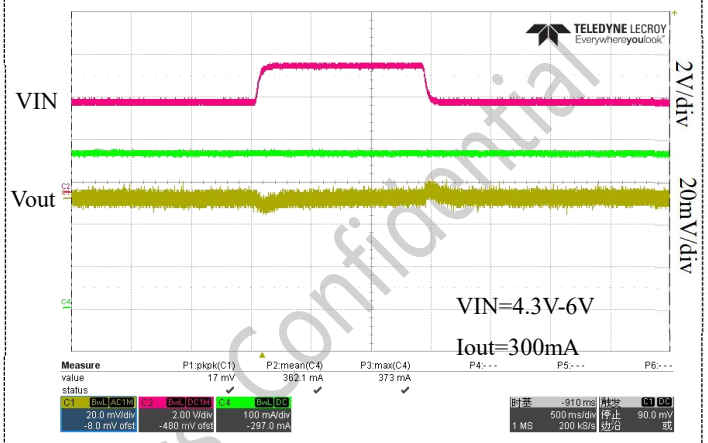


Figure2 VOUT=3.3V Line Transient Response

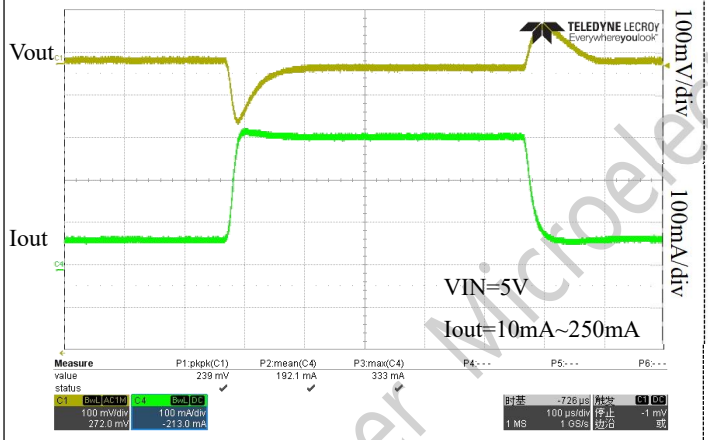


Figure3 Load Transient Response Vout=3.3V

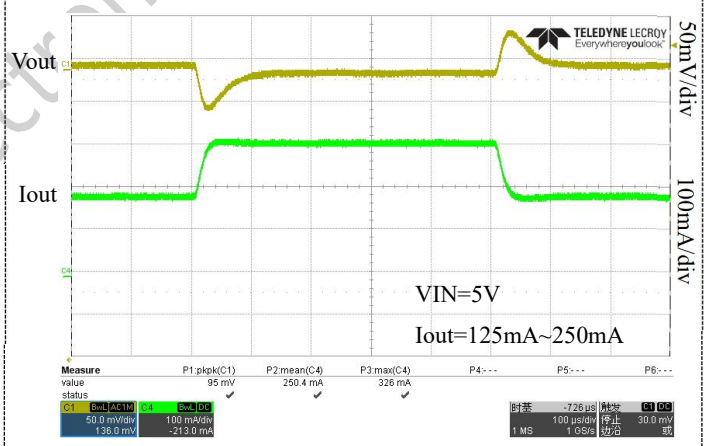


Figure4 Load Transient Response Vout=3.3V

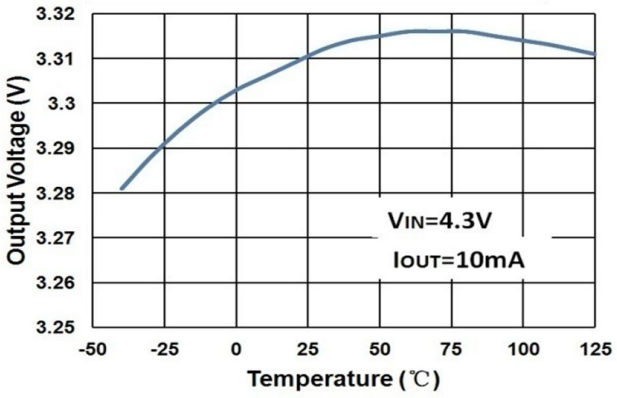


Figure5 Output Voltage vs. Temperature

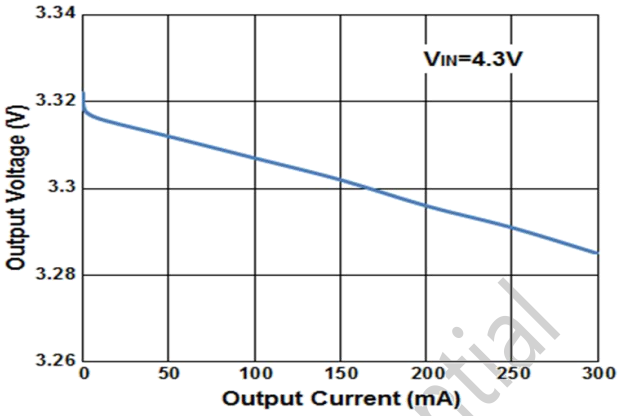


Figure6 Output Current vs Output Current

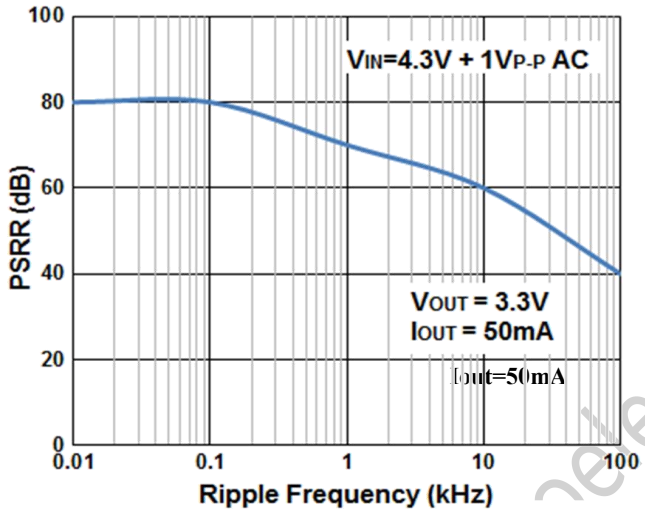


Figure7 Power Supply Rejection Ratio vs. Frequency

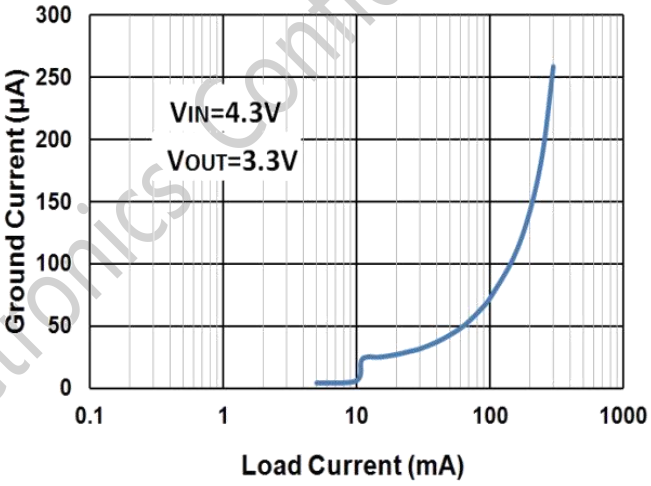


Figure8 Ground Current vs Load Current

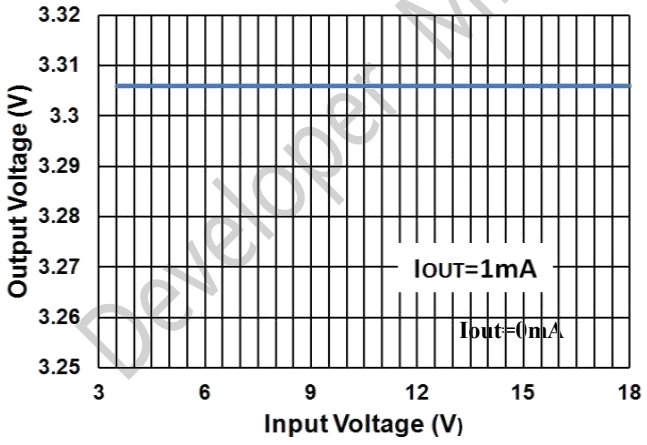


Figure9 Output Voltage vs Input Voltage

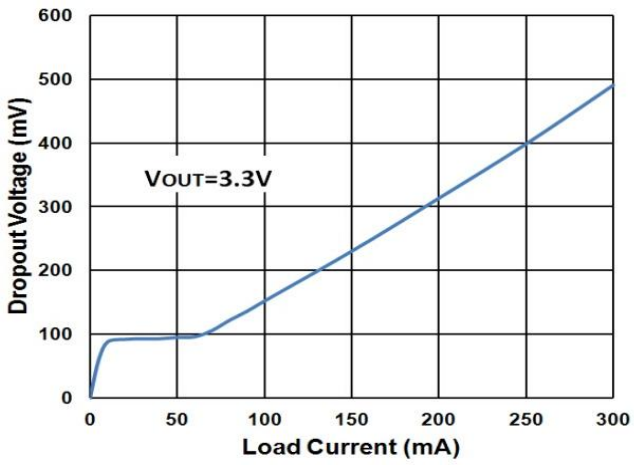


Figure10 Dropout Voltage vs Load Current

Functions Description

- **Feature Description**

The DP31311 series are a group of positive voltage regulators manufactured by CMOS technologies with high ripple rejection, ultra-low noise, low power consumption and low dropout voltage, which can prolong battery life in portable electronics.

The DP31311 series work with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications.

The DP31311 series consume less than 0.1μA in shutdown mode and have fast turn-on time less than 50μS.The series are very suitable for the battery-powered equipment, such as RF applications and other systems requiring a quiet voltage source..

- **Thermal Shutdown**

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160 ° C typically. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

- **Output Current Limit and Short-Circuit Protection**

When overload events happen, the output current is internally limited to 350mA (TYP). When the OUT pin is shorted to ground, the short-circuit protection will limit the output current to 100mA (TYP).

APPLICATION INFORMATION

The DP31311 is a low VIN, ultra-low noise and low dropout LDO and provides 500mA output current.

These features make the device a reliable solution to solve many challenging problems in the generation of clean and accurate power supply.

The high performance also makes the DP31311 useful in a variety of applications. The DP31311 provides the protection functions for output overload, output short-circuit condition and overheating.

The DP31311 provides an EN pin as an external chip enable control to enable/disable the device. When the regulator is in shutdown state, the shutdown current consumes as low as 0.03μA (TYP).

- **Input capacitors selection**

The input decoupling capacitor should be placed as close as possible to the IN pin to ensure the device stability. 1μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance. When VIN is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings.

- **Output capacitors selection**

The output capacitor should be placed as close as possible to the OUT pin. 1μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance. The minimum effective capacitance of COUT that DP31311 can remain stable is 1μF. For ceramic capacitor, temperature, DC bias and package size will change the effective capacitance, so enough margin of COUT must be considered in design. Additionally, COUT with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

- **Enable Operation**

The EN pin of the DP31311 is used to enable/disable its device and to deactivate/activate the output automatic discharge function. When the EN pin voltage is lower than 0.3V, the device is in shutdown state. There is no current flowing from IN to OUT pins. In this state, the automatic discharge transistor is active to discharge the output voltage through a 100Ω (TYP) resistor.

When the EN pin voltage is higher than 0.7V, the device is in active state. The output voltage is regulated to the expected value and the automatic discharge transistor is turned off.

- **PCB Layout**

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance

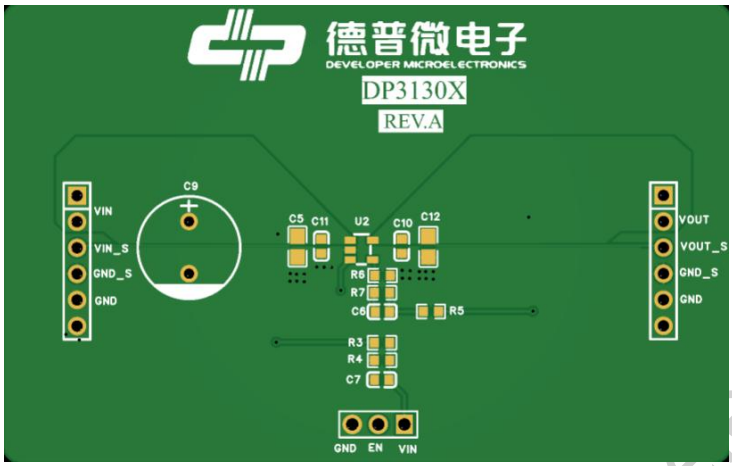
1. The input bypass capacitor C5 and C11 must be placed as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VIN pin to reduce the high frequency injection current.

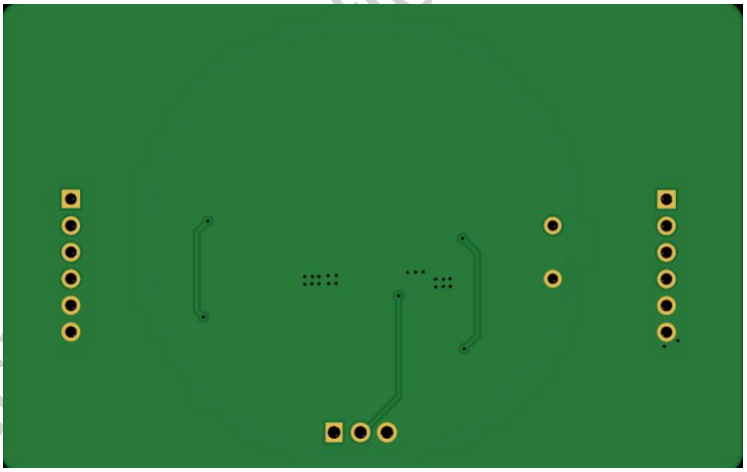
2. The output capacitor, COUT should be placed close to the junction of Vout Pin.

3. The ground connection for C5, C11 and C10, C12 should be as small as possible and connect to system ground plane at only one spot (preferably at the COUT ground point) to minimize injecting noise into system ground plane.

4. Large GND Copper Pour near IC is recommended to minimize the heat of IC.

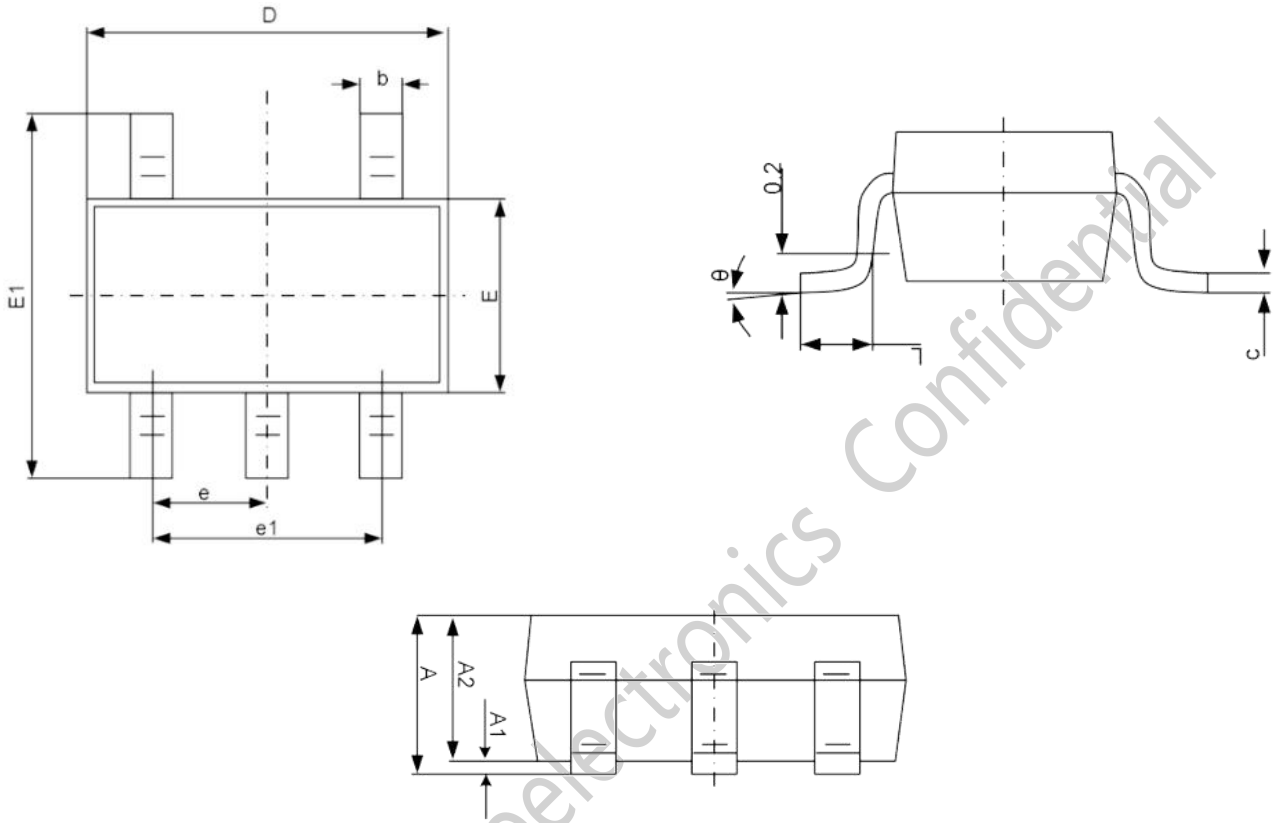
- **Layout Example:**





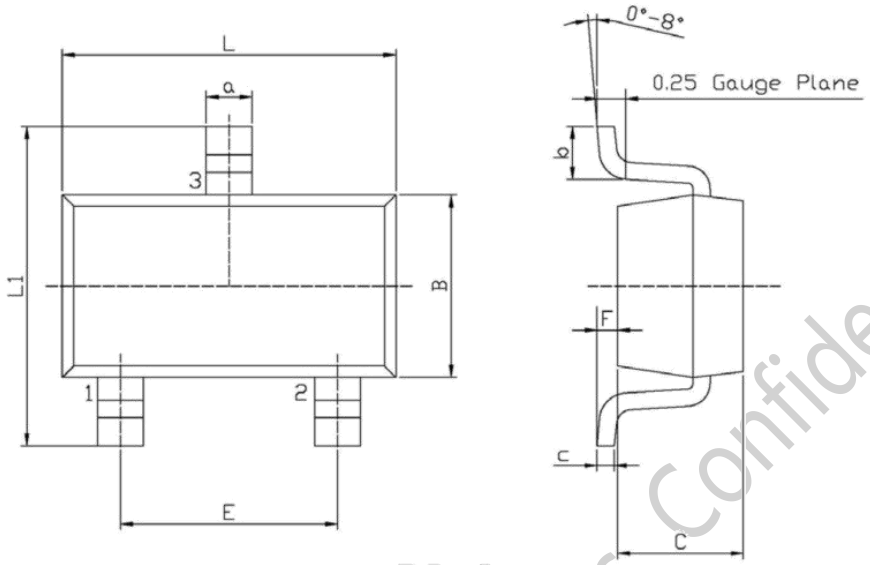
PACKAGE DIMENSION

SOT23-5



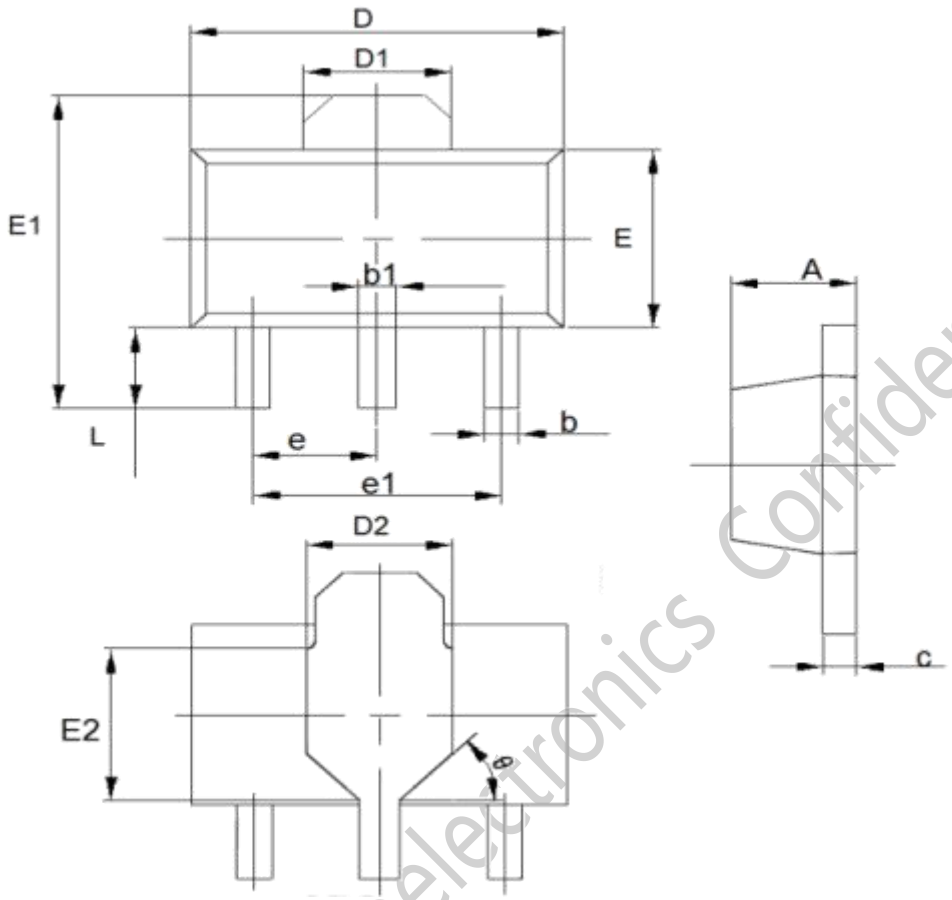
Symbol	Dimensions in Millimeters	
	Min	Max
A	-	1.350
A1	0.000	0.150
A2	1.000	1.200
b	0.300	0.500
c	0.100	0.220
D	2.820	3.020
E	1.500	1.700
E1	2.600	3.000
e	0.950(BSC)	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°

SOT23-3



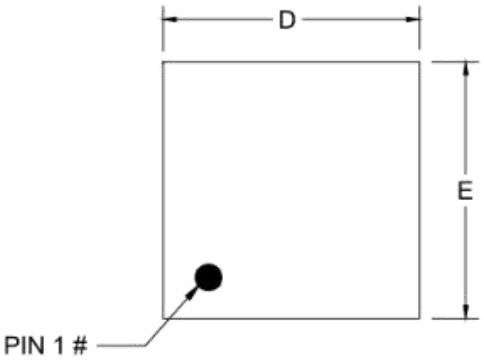
Symbol	Dimensions in Millimeters	
	Min	Max
L	2.82	3.02
B	1.50	1.70
C	0.90	1.30
L1	2.60	3.00
E	1.80	2.00
a	0.35	0.50
c	0.10	0.20
b	0.30	0.55
F	0	0.15

SOT89-3

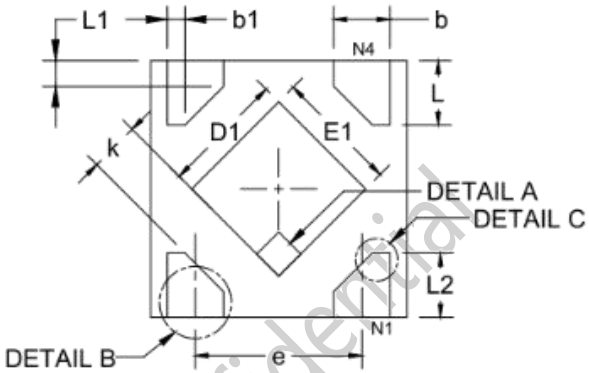


Symbol	Dimensions in Millimeters		Symbol	Dimensions in Millimeters	
	Min	Max		Min	Max
A	1.4	1.6	E1	3.94	4.4
b	0.32	0.52	E2	1.9(TYP)	
b1	0.4	0.58	e	1.5(TYP)	
c	0.35	0.45	L	0.8	1.2
D	4.4	4.6	θ	45°	
D1	1.55(TYP)				
D2	1.75(TYP)				
e1	3.0(TYP)				
E	2.3	2.6			

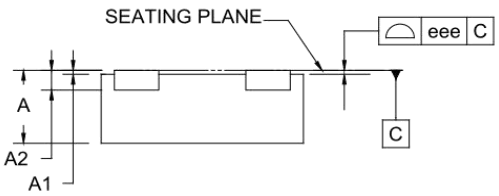
XTDFN_1*1-4L



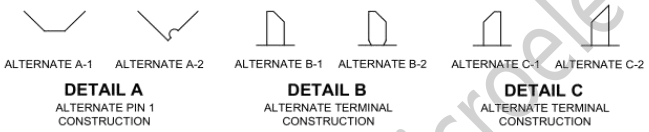
TOP VIEW



BOTTOM VIEW



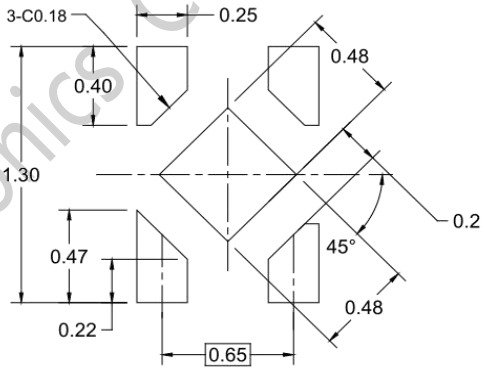
SIDE VIEW



DETAIL A ALTERNATE PIN 1 CONSTRUCTION

DETAIL B ALTERNATE TERMINAL CONSTRUCTION

DETAIL C ALTERNATE TERMINAL CONSTRUCTION



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	Min	MOD	Max
A	0.340	0.370	0.400
A1	0.000	0.020	0.050
A2		0.100REF	
b	0.170	-	0.300
b1		0.068REF	
D	0.950	1.000	1.050
E	0.950	1.000	1.050
D1	0.430	0.480	0.530
E1	0.430	0.480	0.530
e		0.650(BSC)	
L	0.200	0.250	0.300
L1		0.093REF	
L2	0.200	-	0.370
k	0.150	-	-
eee	-	0.050	-

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