# 500mA Ultra-Low Noise Fast RF and High PSRR Linear Regulator

## FEATURES

- Low Dropout Voltage：110mV@100mA
- Low Quiescent Current：50μA(typ.)
- High Ripple Rejection：70dB@1kHz
- Excellent Line and Load Transient Response
- Operating Voltage Range：1.8V～7.0V
- Output Voltage Range：0.6V ～ 5.0V
- High Accuracy：±2%（Typ.）
- Low Output Noise: 40μVRMS (10Hz~100kHz)
- 500mA Output Current
- Built-in Current Limiter, Thermal shutdown and Short-Circuit Protection
- TTL- Logic-Controlled Shutdown Input
- With Output Automatic Discharge
- Available in Green SOT23-5 Packages

## DESCRIPTIONS

The DP31305 seriesare a group of positive voltage regulators manufactured by CMOS technologies with high ripple rejection,ultra low noise, low power consumption and low dropout voltage, which can prolong battery life in portable electronics.

The DP31305 series work with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications.

The DP31305 series consume less than 0.1 μ A inshutdown mode and have fast turn-on time less than 50 μ s.The series are very suitable for the battery-powered equipments, such as RF applicationsand other systems requiring a quiet voltage source.

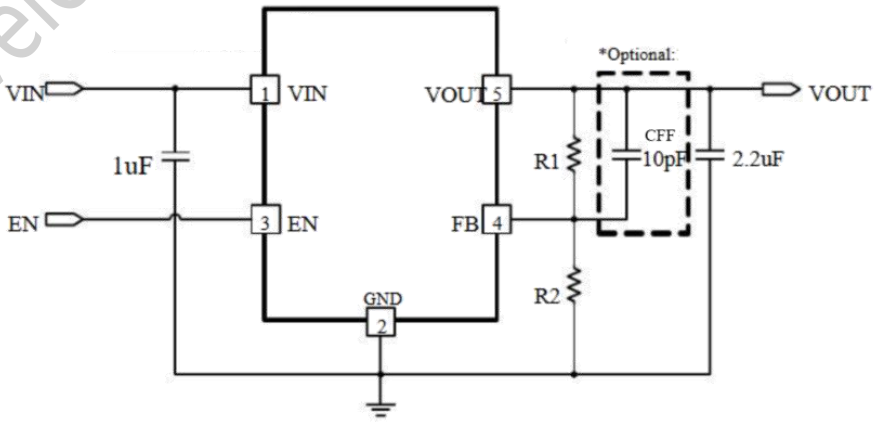
## APPLICATIONS

- RF: VCOs, Receivers, ADC
- Cellular and Cordless Telephones
- IP Cameras
- Wireless LAN Devices
- Handheld Organizers
- Audio
- Tablet, MID

## ORDERING INFORMATION

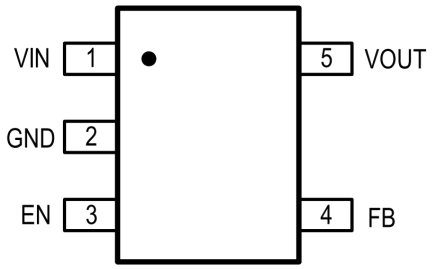
| Part Number | Description |
|---|---|
| SOT23-5 | Pb free in T&R, 3000 Pcs/Reel |

## TYPICAL APPLICATION CIRCUIT



# PRODUCT DESCRIPTION

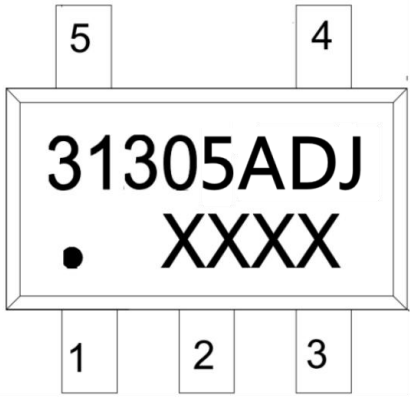
## ➢ Pin Arrangement




## ➢ Pin Configuration

| SOT23-5 | Pin Name | Description |
|---|---|---|
| 1 | IN | Input Supply Voltage Pin. It is recommended to use a 1μF or larger ceramic capacitor from IN pin to ground to get good power supply decoupling. This ceramic capacitor should be placed as close as possible to IN pin. |
| 2 | GND | Ground. |
| 3 | EN | Enable Pin. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. This pin must be pulled high by an external resistor connected to IN pin if EN pin is not used. |
| 4 | FB | Feedback pin. Feedback voltage is set to be 0.6V. FB pin for adjustable output option |
| 5 | OUT | Regulator Output Pin. It is recommended to use a ceramic capacitor with effective capacitance in the range of 1μF to 10μF to ensure stability. This ceramic capacitor should be placed as close as possible to OUT pin. |

## ➢ Marking Information




DP31305 for product name:

XXXX The first X represents the last year,2020 is 0;The second X represents the month,inA-L 12 letters;The third and fourth X on behalf of the date,01-31said;

| Marking | Model | VOUT Voltage | PACKAGE |
|---|---|---|---|
| 31305ADJ | DP31305-ADJAST | Adjustable | SOT23-5 |

## ➢ Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)(1)

| PARAMETER | Min | Max | Unit |
|---|---|---|---|
| VIN Voltage(1) | -0.3 | 8 | V |
| EN Voltage | -0.3 | 8 | V |
| VOUT Voltage(2) | -0.3 | VIN+0.3 | V |
| Output Current | - | 500 | mA |
| Power Dissipation | - | 400 | mW |
| Operating free air temperature range | -40 | 85 | ℃ |
| Operating junction temperature,TJ | -40 | 150 | ℃ |
| Storage temperature, Tstg | -65 | 150 | ℃ |
| Lead Temperature（Soldering，10sec.) | - | 260 | ℃ |

Note:(1)Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute – maximum – rated conditions for extended periods may affect device reliability.

（2）All voltage values are with respect to network ground terminal

## ➢ Recommended Operating Conditions

| PARAMETER | Min | Max | Unit |
|---|---|---|---|
| VIN Voltage($V_{IN}$) | 1.8 | 7 | V |
| VOUT Voltage($V_{OUT}$) | 0.6 | 5.5 | V |
| Output current($I_{OUT}$) | - | 500 | mA |
| TJ | -40 | 125 | ℃ |

Note : (1)All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

## ➢ ESD Ratings

| PARAMETER | Description | Value | Unit |
|---|---|---|---|
| HBM | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| CDM | Charged-device model (CDM), per JEDEC specification JESD22-C101 | ±200 | V |

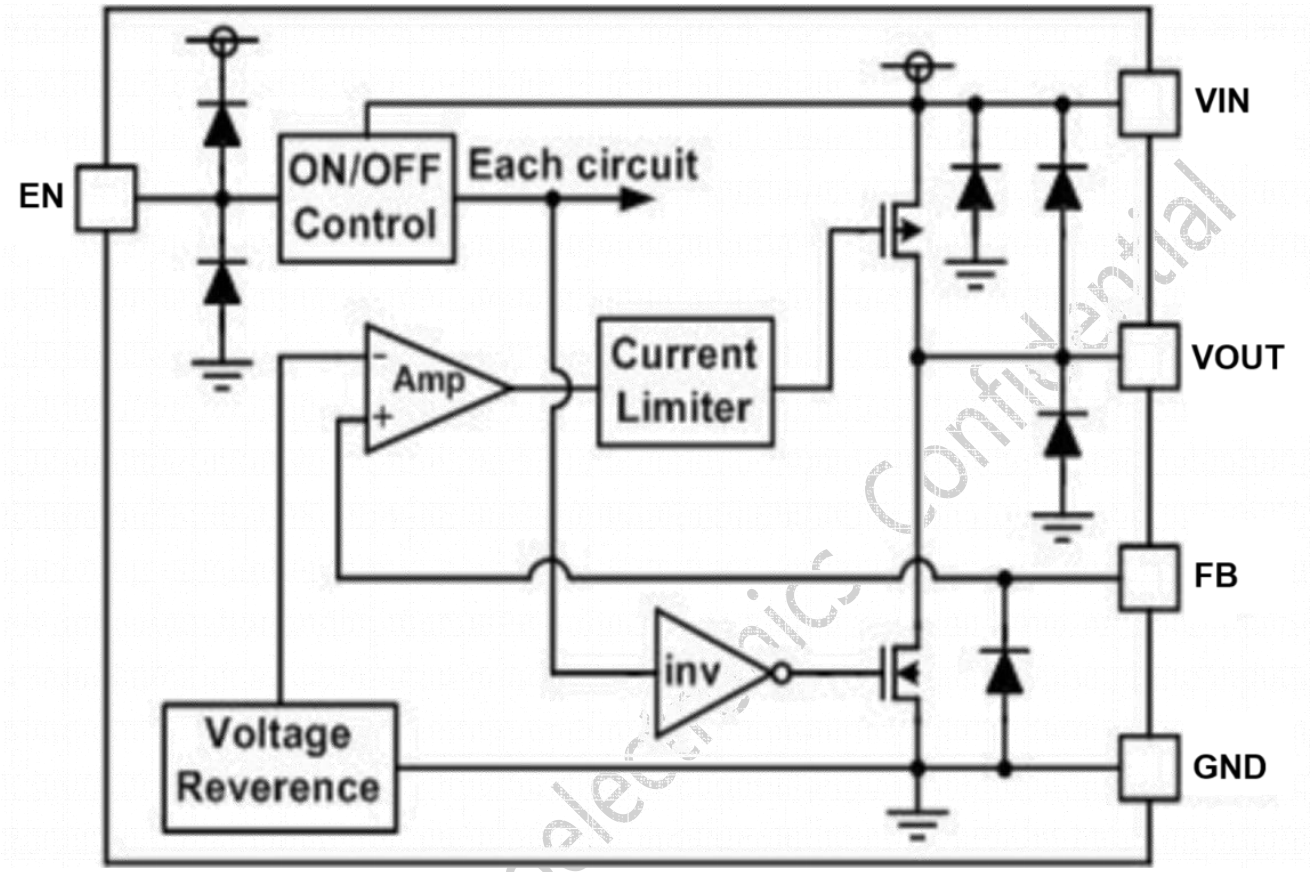
Note : (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## ➢ Thermal Information

| THERMAL METRIC | Description | SOT23-5 | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance(1)(2) | 191.6 | ℃/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 141.4 | ℃/W |
| $R_{\theta JB}$ | Junction-to-board(Bottom) thermal resistance | 44.5 | ℃/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 34.5 | ℃/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 43.9 | ℃/W |

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.
Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

## BLOCK DIAGRAM



# ELECTRICAL CHARACTERISTICS

**$V_{IN}$=$V_{OUT}$+1V, $C_{IN}$=$C_{OUT}$=1μF，$T_A$=25℃,unless otherwise specified**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input Voltage | $V_{IN}$ | - | 1.8 | - | 7 | V |
| Supply Current | IQ | $I_{OUT}$=0mA | | 45 | 90 | uA |
| Standby Current | ISHDN | $V_{EN}$=0V | | 0.1 | 1 | uA |
| FB Voltage | VFB | IOUT=1mA | 0.588 | 0.600 | 0.612 | V |
| FB pin current | | VFB=1.8V | | | 1 | μA |
| Output Current | $I_{OUT}$ | - | | 500 | | mA |
| Dropout Voltage | VDROP | Iout=60mA Vout=2.8V | | 70 | | mV |
| | | Iout=100mA Vout=2.8V | | 120 | | mV |
| | | Iout=200mA Vout=2.8V | | 250 | | mV |
| | | Iout=300mA Vout=2.8V | | 360 | | mV |
| | | Iout=400mA Vout=2.8V | | 500 | | mV |
| | | Iout=500mA Vout=2.8V | | 650 | | mV |
| Load Regulation | $\Delta V_{OUT}$ | $V_{IN}$= $V_{OUT}$ +1V, 1mA≤$I_{OUT}$≤500mA | | 10 | | mV |
| Line Regulation | $\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$ | $I_{OUT}$ =100mA $V_{OUT}$ +1V≤$V_{IN}$≤6V | | 0.01 | 0.2 | %/V |
| Output Voltage Temperature Characteristics | $\frac{\Delta V_{OUT}}{\Delta T \times V_{OUT}}$ | $I_{OUT}$ =10mA -40≤T≤+85℃ | | 50 | | ppm |
| Current Limit | $I_{LIM}$ | | | 600 | | mA |
| Short Current | Ishort | $V_{OUT}$=0V | | 20 | | mA |
| Power Supply Rejection Rate | PSRR | F=100HZ Iout=50mA | | 80 | | dB |
| | | F=1KHZ Iout=50mA | | 70 | | |
| | | F=10KHZ Iout=50mA | | 50 | | |
| EN Rising Threshold | $V_{EN(R)}$ | 1.8V≦VIN≦5.5V | 1.5 | | | V |
| EN Falling Threshold | $V_{EN(F)}$ | 1.8V≦VIN≦5.5V | | | 0.3 | V |
| Over-Temperature Protection | TSD | | | 160 | | ℃ |
| Over-Temperature Protection hysteresis | △TSD | | | 20 | | ℃ |

# TYPICAL CHARACTERISTICS

TJ = +25℃, VIN = (VOUT(NOM) + 1V) (whichever is greater), VEN = VIN, CIN = COUT = 1μF, unless otherwise noted.

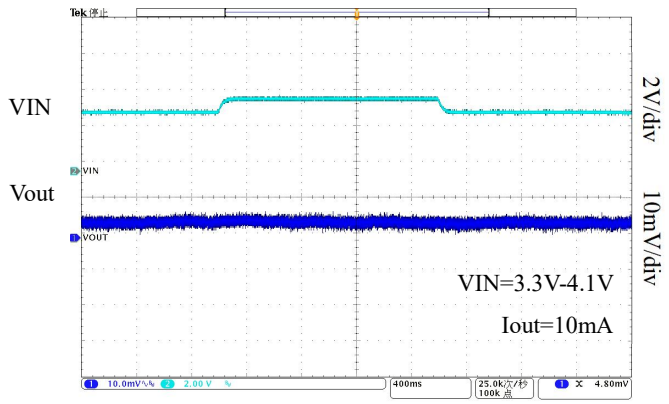



**Figure1 Vout=2.8V Line Transient Response**

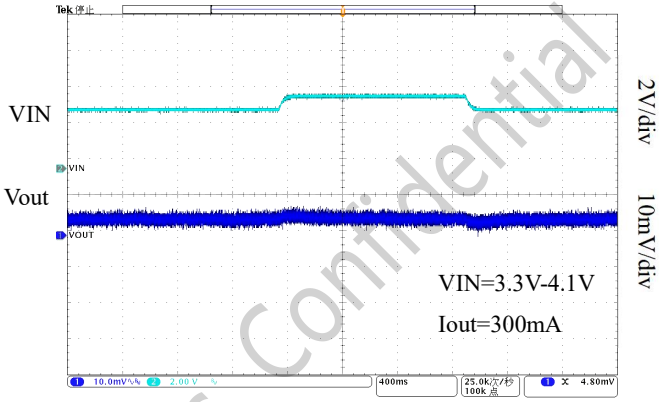



**Figure2 VOUT=2.8V Line Transient Response**

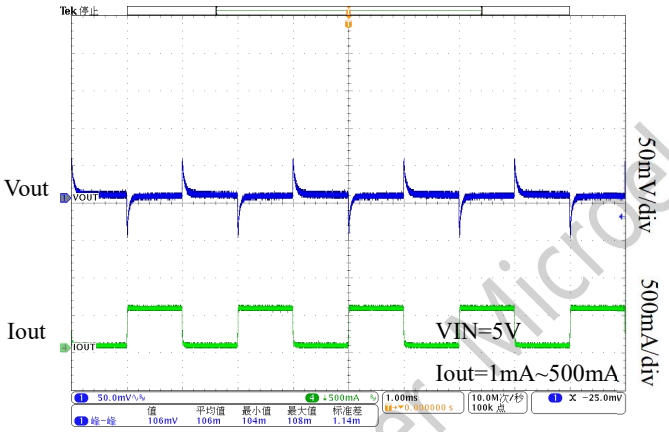



**Figure3 Load Transient Response Vout=2.8V**

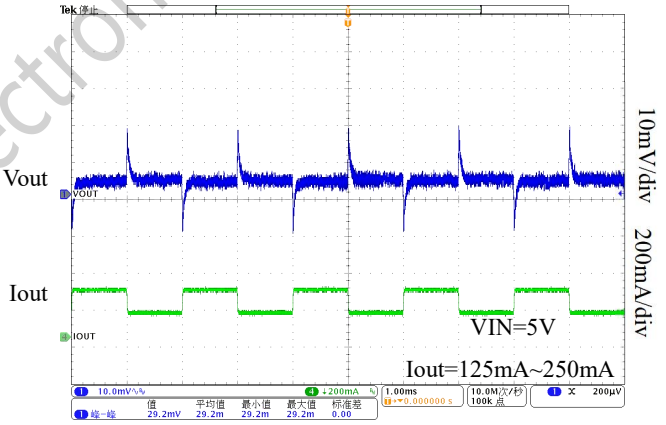



**Figure4 Load Transient Response Vout=2.8V**

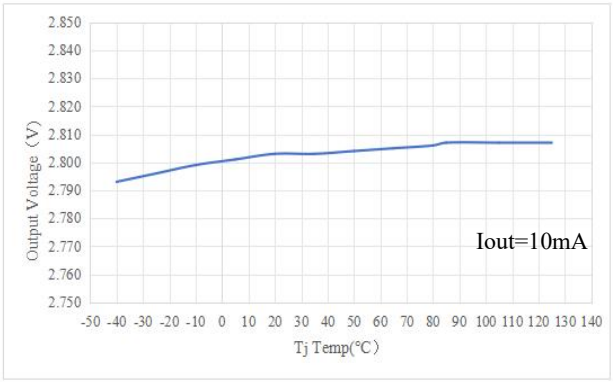



Figure5 Output Voltage vs. Temperature

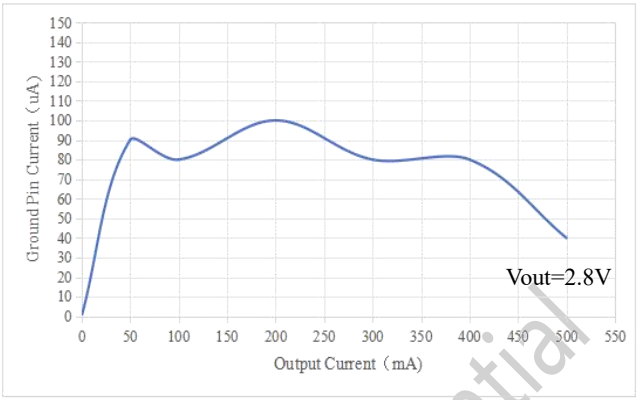



Figure6 Output Current vs Ground Current

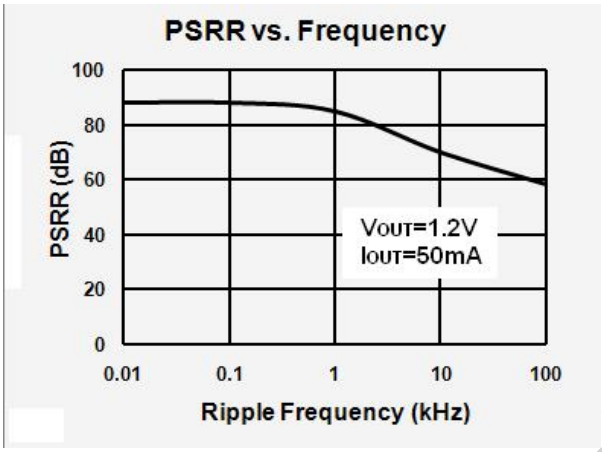



Figure7 Power Supply Rejection Ratio vs. Frequency

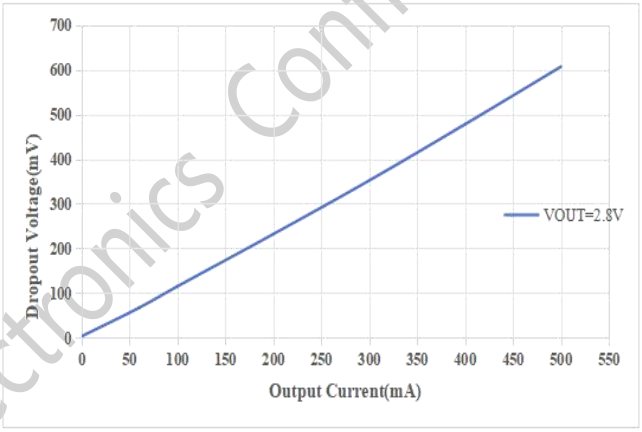



Figure8 Dropout vs Output Current

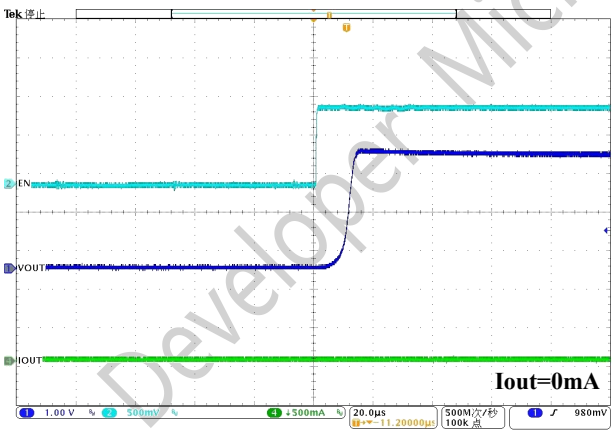



Figure9 EN Start Up with Load

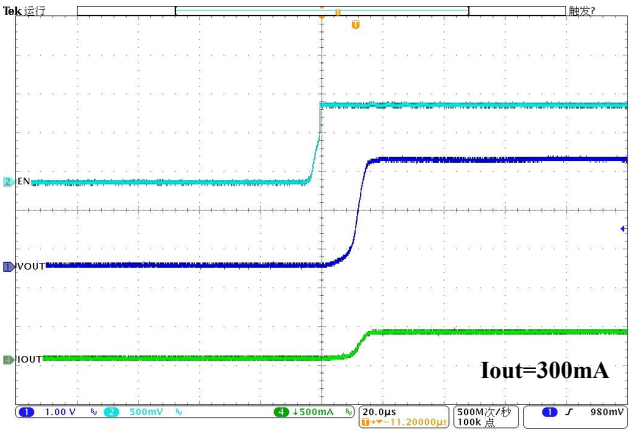



Figure10 EN Start Up with Load

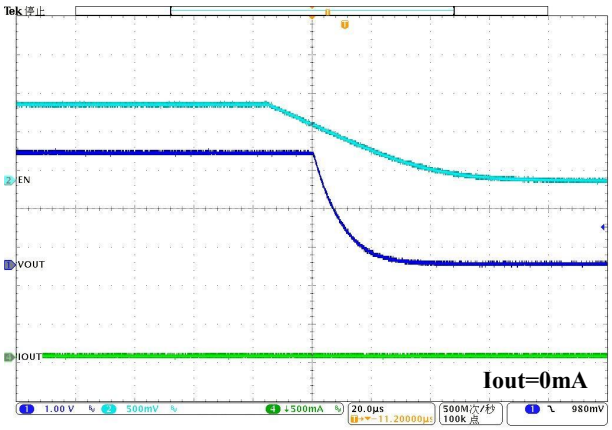



Figure11 EN Start Down with Load

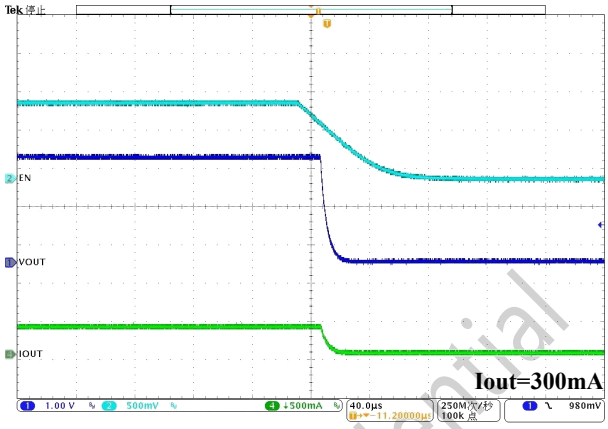



Figure12 EN Start Down with Load

# FUNCTIONS DESCRIPTION

- **Feature Description**

The DP31305 series are a group of positive voltage regulators manufactured by CMOS technologies with high ripple rejection, ultra-low noise, low power consumption and low dropout voltage, which can prolong battery life in portable electronics.

The DP31305 series work with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications.

The DP31305 series consume less than 0.1μA in shutdown mode and have fast turn-on time less than 50μS.The series are very suitable for the battery-powered equipment, such as RF applications and other systems requiring a quiet voltage source..

- **Thermal Shutdown**

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160 ° C typically. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

- **Output Current Limit and Short-Circuit Protection**

When overload events happen, the output current is internally limited to 600mA (TYP). When the OUT pin is shorted to ground, the short-circuit protection will limit the output current to 20mA (TYP).

# APPLICATION INFORMATION

The DP31305 is a low VIN, ultra-low noise and low dropout LDO and provides 500mA output current.

These features make the device a reliable solution to solve many challenging problems in the generation of clean and accurate power supply.

The high performance also makes the DP31305 useful in a variety of applications. The DP31305 provides the protection functions for output overload, output short-circuit condition and overheating.

The DP31305 provides an EN pin as an external chip enable control to enable/disable the device. When the regulator is in shutdown state, the shutdown current consumes as low as 0.03μA (TYP).

- **Input capacitors selection**

The input decoupling capacitor should be placed as close as possible to the IN pin to ensure the device stability. 1μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance. When VIN is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings.

- **Output capacitors selection**

The output capacitor should be placed as close as possible to the OUT pin. 1μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance. The minimum effective capacitance of COUT that DP31305 can remain stable is 1μF. For ceramic capacitor, temperature, DC bias and package size will change the effective capacitance, so enough margin of COUT must be considered in design. Additionally, COUT with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

- **Enable Operation**

The IC's internal circuitry can be shutdown via the signal from the EN pin with the DP31305-ADJ series. Driving EN over 1.2 V turns on the regulator. Driving EN below 0.3 V puts the regulator into shutdown mode.

- **Setting The Output Voltage**

Figure 1 shows the typical application circuit with DP31305. The external resistor sets the output voltage according to the following equation:

$$V_{OUT} = 0.6V \times \left(1 + \frac{R1}{R2}\right)$$

Table 1.Resistor select for output voltage setting

| VOUT | R1 | R2 | Cff |
|---|---|---|---|
| 1.2V | 30.1K | 30.1K | Opt. |
| 1.5V | 45.3K | 30.1K | Opt. |
| 1.8V | 60.4K | 30.1K | Opt. |
| 2.5V | 95.3K | 30.1k | Opt. |
| 2.8V | 110K | 30.1k | Opt. |
| 3.0V | 120K | 30.1K | Opt. |
| 3.3V | 137K | 30.1K | Opt. |
| 5.0V | 221K | 30.1k | Opt. |

- **PCB Layout**

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance

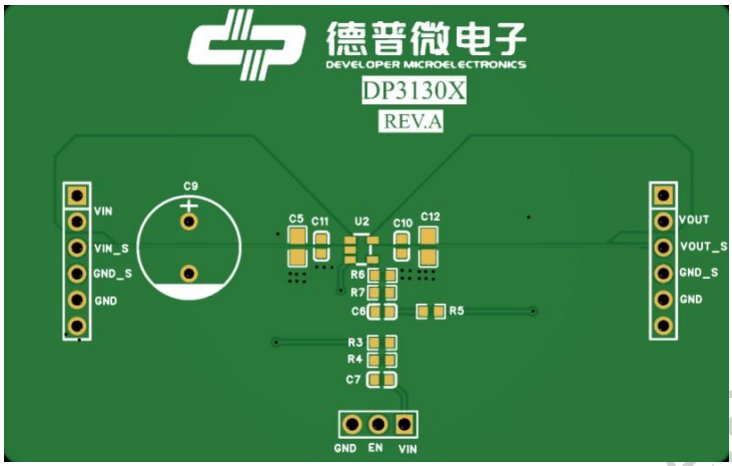
**1.** The input bypass capacitor C5 and C11 must be placed as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VIN pin to reduce the high frequency injection current.

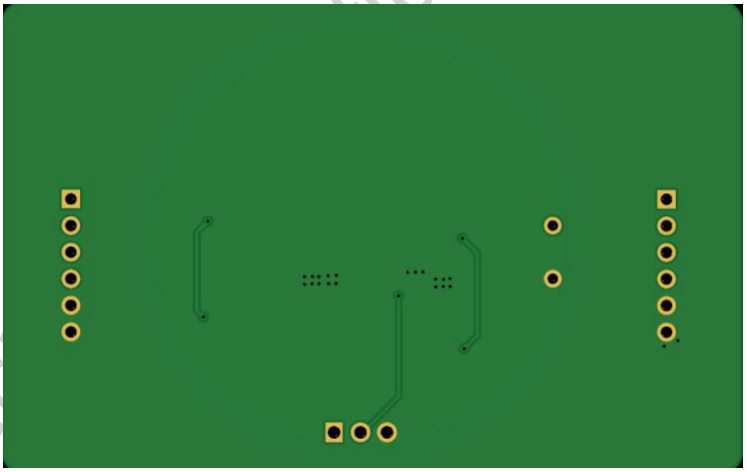
**2.** The output capacitor, COUT should be placed close to the junction of Vout Pin.

**3.** The ground connection for C5, C11 and C10, C12 should be as small as possible and connect to system ground plane at only one spot (preferably at the COUT ground point ) to minimize injecting noise into system ground plane.

**4**. Large GND Copper Pour near IC is recommended to minimize the heat of IC.

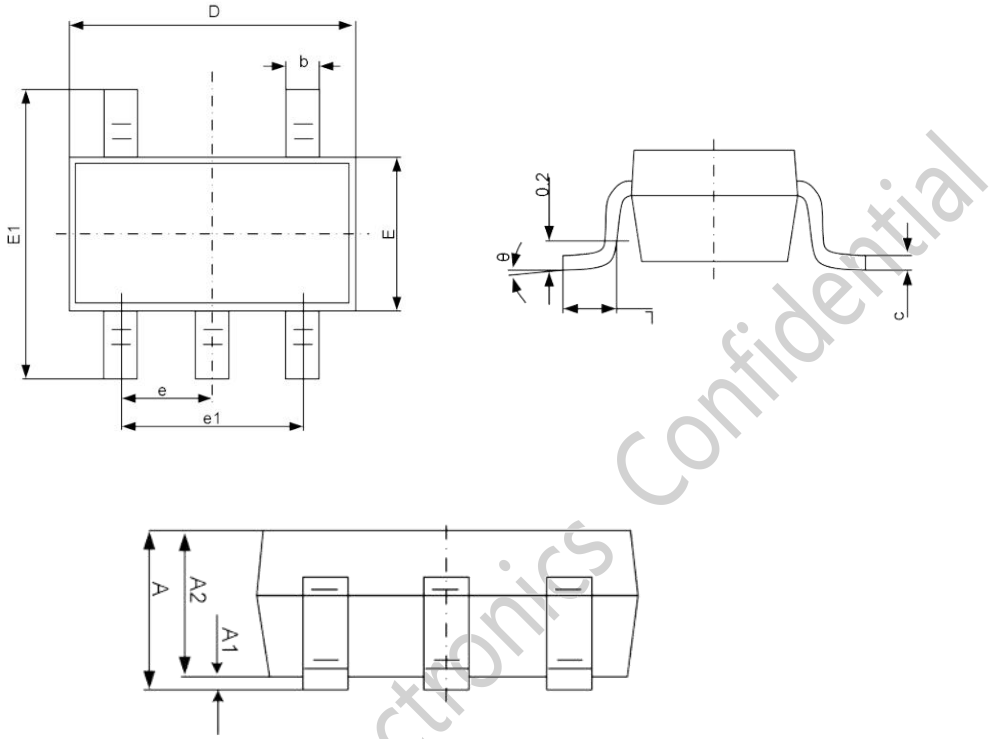
- **Layout Example:**



# PACKAGE DIMENSION

## SOT23-5




| Symbol | Dimensions in Millimeters | |
|---|---|---|
| | Min | Max |
| A | - | 1.350 |
| A1 | 0.000 | 0.150 |
| A2 | 1.000 | 1.200 |
| b | 0.300 | 0.500 |
| c | 0.100 | 0.220 |
| D | 2.820 | 3.020 |
| E | 1.500 | 1.700 |
| E1 | 2.600 | 3.000 |
| e | 0.950(BSC) | |
| e1 | 1.800 | 2.000 |
| L | 0.300 | 0.600 |
| θ | 0° | 8° |

# REVISION HISTORY

| Editions | Revised Date | Redaction person | Revision content |
|---|---|---|---|
| REV1.0 | 2024/12/23 | PXB | First release |
| | | | |
| | | | |

# OFFICIAL ANNOUNCEMENT

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