

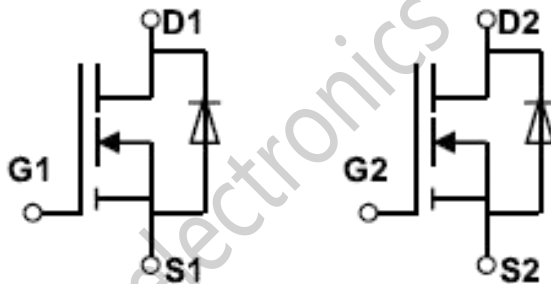
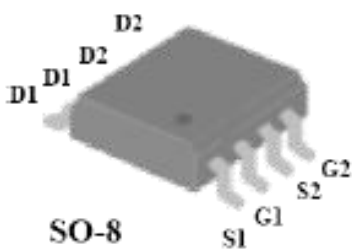
FEATURES

- Super high dense cell design for low RDS(ON)
- Rugged and reliable
- Simple drive requirement
- SOP-8 package

PRODUCT SUMMARY		
VDSS	ID	RDS(ON)(mΩ)Typ
20V	6A	22@VGS=4.5V
		35@VGS=2.5V



NOTE:The 9926 is available
In a lead-free package



FXXX The F represents fixed ,the first X represents the last year,2014 is 4;The second X represents the week,inA-G 7 letters; The last X represents the wafer batch code

ABSOLUTE MAXIMUM RATINGS (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	±12	V
Drain Current-Continuous @ T _J =25°C	I _D	6	A
Pulsed ^b	I _{DM}	20	A
Drain-Source Diode Forward Current ^a	I _S	1.7	A
Maximum Power Dissipation ^a	P _D	2.5	W
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 To 150	°C

THERMAL CHARACTERISTIC

Parameter	Symbol	Limit	Unit
Thermal rResistance,Junction-to-Ambient ^a	R _{θJA}	80	°C/W

ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	20	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-16V V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±8V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	0.5	0.8	1.5	V
Drain-Source On-State	R _{DS(ON)}	V _{GS} =-4.5V, I _D =6A	-	22	25	mΩ

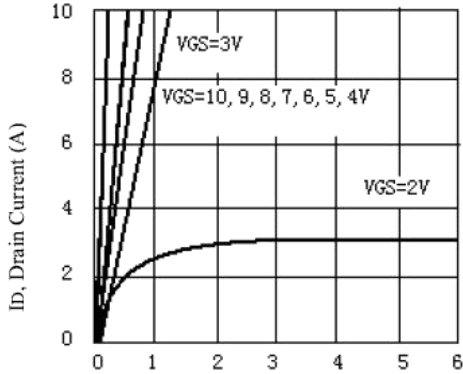
N-Channel Enhancement Mode Field Effect Transistor

Resistance		$V_{GS}=2.5V, I_D=2.8A$	-	35	38	
Forward Transconductance	g_{FS}	$V_{GS}=5V, I_D=5A$	-	5	-	S
Dynamic Characteristics						
Input Capacitance	C_{ISS}	$V_{DS}=-10V,$ $V_{GS}=0V, F=1.0MHz$	-	608	-	pF
Output Capacitance	C_{OSS}		-	115	-	
Reverse Transfer Capacitance	C_{RSS}		-	86	-	
Switching Characteristics^b						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V,$ $I_D=6A$ $V_{GS}=-4.5V, R_{GEN}=10\Omega,$ $R_L=10\Omega$	-	10	-	nS
Turn-on Rise Time	t_r		-	14	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	39	-	nS
Turn-Off Fall Time	t_f		-	26	-	nS
Total Gate Charge	Q_g	$V_{DD}=10V,$ $I_D=-1A,$ $V_{GS}=4.5V$	-	9.2	-	nC
Gate-Source Charge	Q_{gs}		-	1.6	-	nC
Gate-Drain Charge	Q_{gd}		-	2.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=-1.7A$	-	0.848	-1.3	V

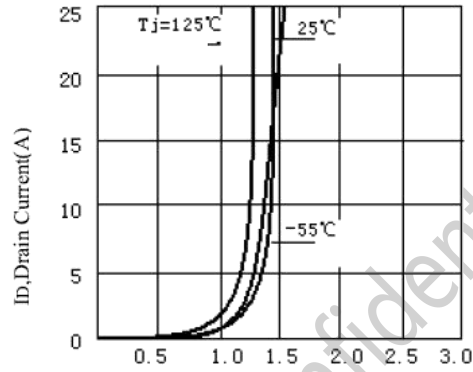
Note:

- Surface mounted on FR4 Board, $t \leq 10\text{sec}$
- Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
- Guaranteed by design, not subject to production testing.

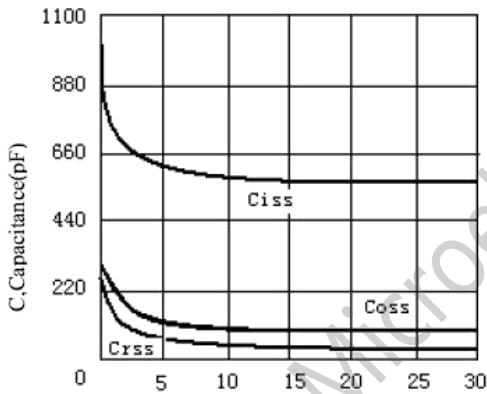
CHARACTERIZATION PLOTS



Vds, Drain-to-Source Voltage (V)
Figure 1. Output Characteristics



VGS, Gate-to-source Voltage (V)
Figure 2. Transfer Characteristics



VGS, Drain-to-Source Voltage
Figure 3. Capacitance

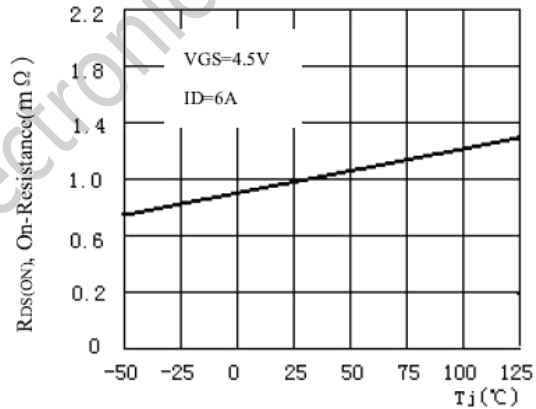
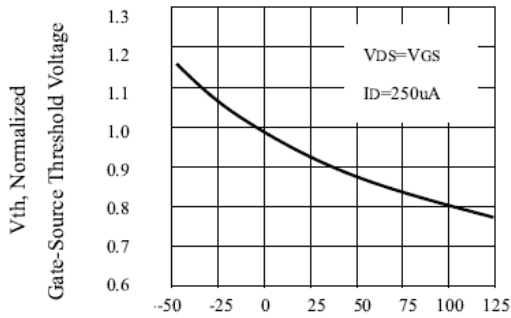


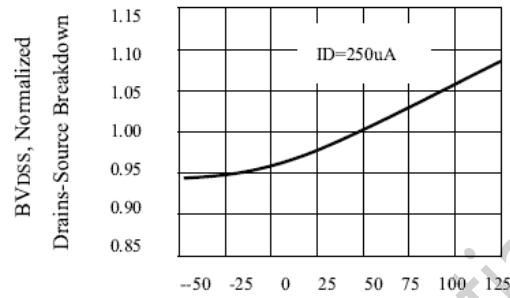
Figure 4. On-Resistance Variation with Temperature



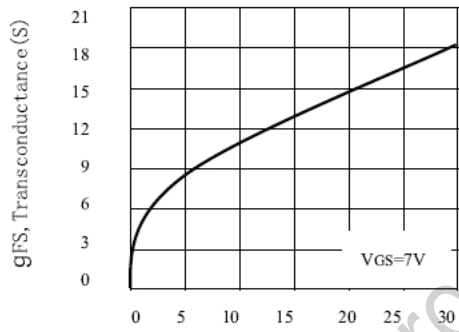
N-Channel Enhancement Mode Field Effect Transistor



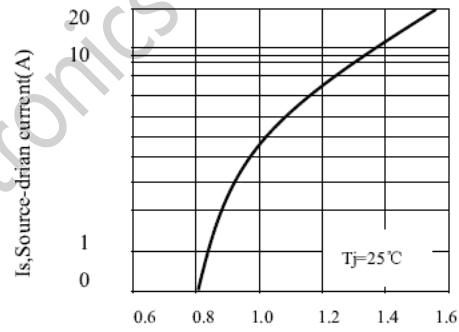
Tj, Junction Temperature (°C)
Figure 5. Gate Threshold Variation With Temperature



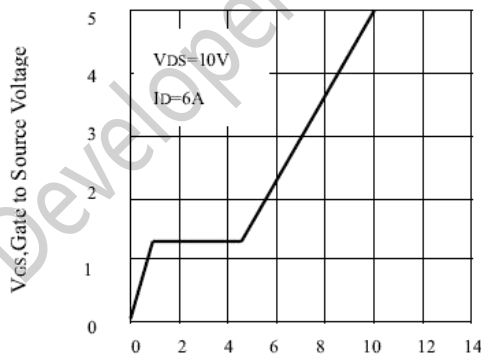
Tj, Junction Temperature (°C)
Figure 6. Breakdown Voltage Variation With Temperature



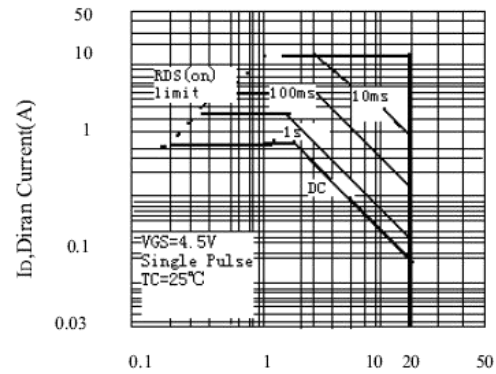
IDS, Drain-Source Current (A)
Figure 7. Transconductance Variation With Drain Current



VSD, Body Diode Forward Voltage
Figure 8. Body Diode Forward Voltage Variation with Source Current



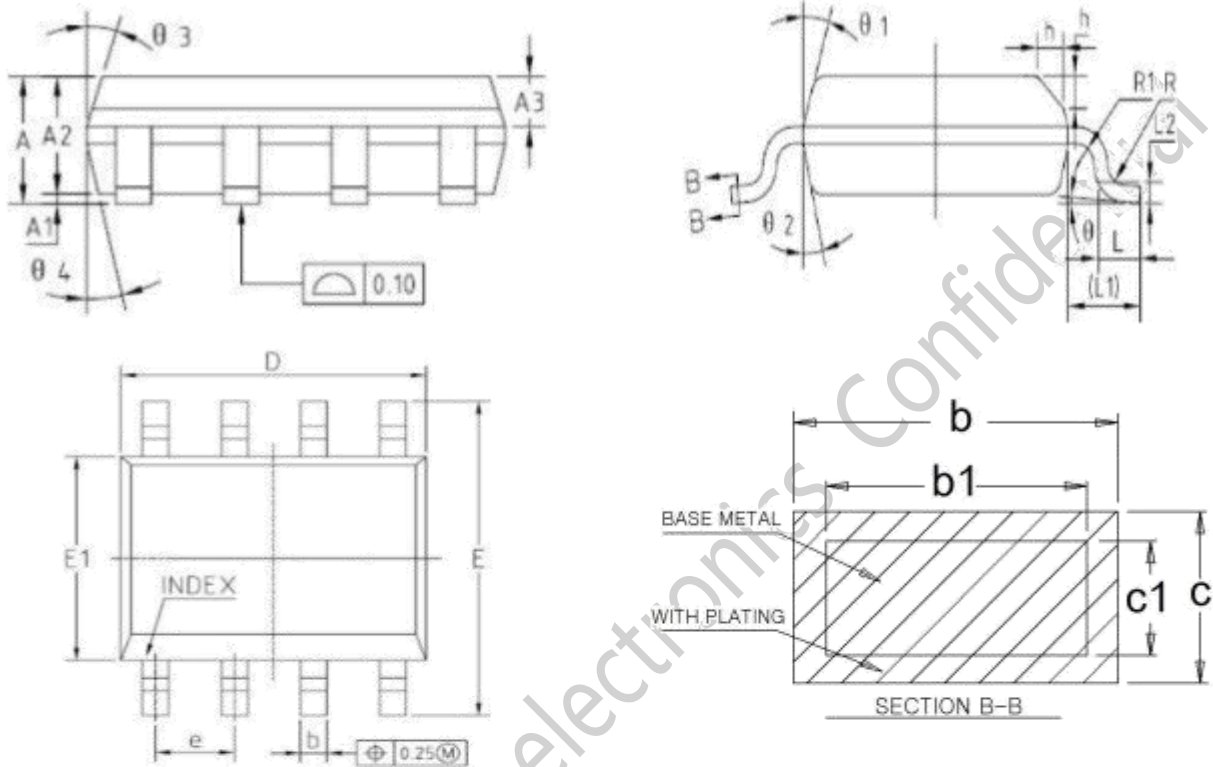
Qg, Total Gate Charge (nC)
Figure 9. Gate Charge



VDS, Drain-Source Voltage (V)
Figure 10. Maximum Safe Operating Area

PACKAGE OUTLINE

SOP8



Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	1.45	1.55	1.65
A1	0.10	0.15	0.20
A2	1.353	1.40	1.453
A3	0.55	0.60	0.65
b	0.38	-	0.51
b1	0.37	0.42	0.47
c	0.17	-	0.25
c1	0.17	0.20	0.23
D	4.85	4.90	4.95
E	5.85	6.00	6.15
E1	3.85	3.90	3.95
e	1.245	1.27	1.295
L	0.45	0.60	0.75
L1	-	1.050REF	-
L2	-	0.250BSC	-
Ø1-Ø4	12° REF		
h	0.40REF		
R	0.15° REF		
R1	0.15° REF		

OFFICIAL ANNOUNCEMENT

Division I will ensure the accuracy and reliability of the product specification document, but we reserve the right to independently modify the content of the specification document without prior notice to the customer. Before placing an order, customers should contact us to obtain the latest relevant information and verify that this information is complete and up-to-date. All product sales are subject to the sales terms and conditions provided by our company at the time of order confirmation.

Division I will periodically update the content of this document. Actual product parameters may vary due to differences in models or other factors. This document does not serve as any express or implied guarantee or authorization.

The product specification does not include any authorization for the intellectual property owned by our company or any third party. With respect to the information contained in this product specification, we make no explicit or implied warranties, including but not limited to the accuracy of the specification, its fitness for commercial use, suitability for specific purposes, or non-infringement of our company's or any third party's intellectual property. We also do not assume any responsibility for any incidental or consequential losses related to this specification document and its use.

We do not assume any obligations regarding application assistance or customer product design. Customers are responsible for their own use of our company's products and applications. In order to minimize risks associated with customer products and applications, customers should provide thorough design and operational safety validation.

The reproduction, transmission or use of this document or its contents is not permitted without express written authority. Once discovered, the company will pursue its legal responsibility according to law and compensate for all losses caused to the company.

Please note that the product is used within the conditions described in this document, paying particular attention to the absolute maximum rating, operating voltage range, and electrical characteristics. The Company shall not be liable for any damage caused by malfunctions, accidents, etc. caused by the use of the product outside the conditions stated in this document.

Division I has been committed to improving the quality and reliability of products, but all semiconductor products have a certain probability of failure, which may lead to some personal accidents, fire accidents, etc. When designing products, pay full attention to redundancy design and adopt safety indicators, so as to avoid accidents.

When using our chips to produce products, Division I shall not be liable for any patent dispute arising from the use of the chip in the product, the specification of the product, or the country of import, etc., in the event of a patent dispute over the products including the chip.