30V, Ultra-Low 2uA I_Q，Low Noise LDO Regulators

FEATURES

- Low Dropout Voltage：550mV@100mA
- Low Quiescent Current：2μA(typ.)
- High Ripple Rejection：65dB@1kHz
- Operating Voltage Range：4.5V～30V
- Fix Output Voltage：2V、2.4V、2.8V、3V、3.3V、3.6V、4V、4.4V、5.0V
- High Accuracy：±2% （Typ.)
- Low Output Noise: 27xV_{OUT} μV_{RMS} (10Hz~100kHz)
- 250mA Output Current
- Built-in Thermal shutdown and Short-Circuit Protection
- Available in Green SOT89-3 、SOT23-3 Packages

DESCRIPTIONS

The DP31331 series are a group of positive voltage regulators manufactured by CMOS technologies with low power consumption and low dropout voltage, which provide large output currents even when the difference of the input-output voltage is small.

The DP31331 series can deliver 300mA output current and allow an input voltage as high as 18V. The series are very suitable for the battery-powered equipments, such as RF applications and other systems requiring a quiet voltage source.

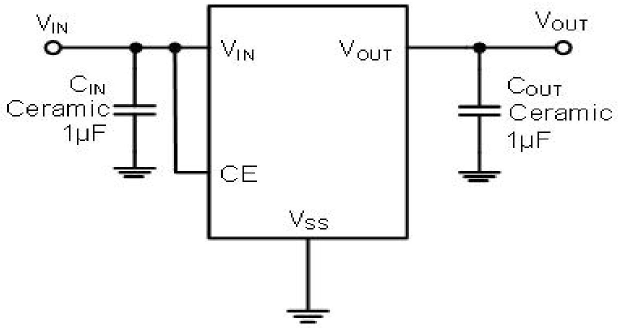
APPLICATIONS

- Power Meter
- Multicell Battery Powered Equipment
- Communication equipment
- Smoke Detector
- Audio/Video Equipment
- LED Driver

ORDERING INFORMATION

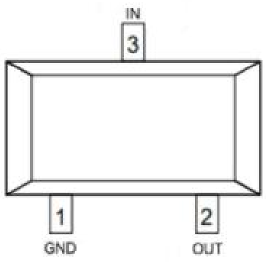
Part Number	Description
SOT23-3	Pb free in T&R, 3000 Pcs/Reel
SOT89-3	Pb free in T&R, 1000 Pcs/Reel

TYPICAL APPLICATION CIRCUIT

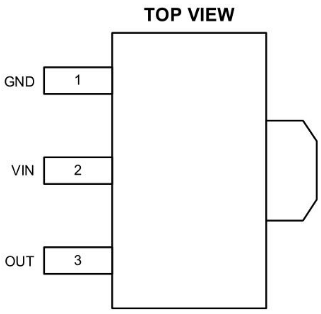


PRODUCT DESCRIPTION

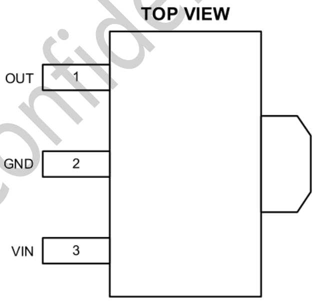
➢ Pin Arrangement



SOT-23-3



SOT89-3A

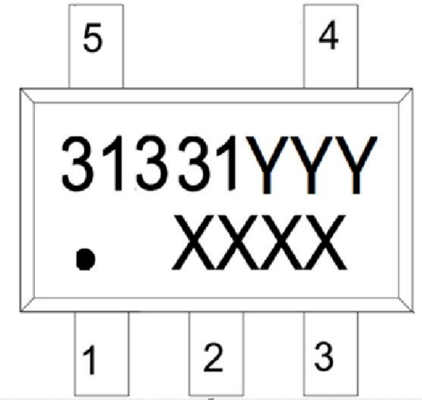


SOT89-3B

➢ Pin Configuration

SOT23-3	SOT89-3A	SOT89-3B	Pin Name	Description
1	1	2	GND	Ground.
2	2	3	VIN	Input Supply of the LDO.
3	3	1	OUT	Regulator Output Pin. It is recommended to use a ceramic capacitor with effective capacitance in the range of 2.2μF to 10μF to ensure stability. This ceramic capacitor should be placed as close as possible to OUT pin.

➢ Marking Information



DP31331 for product name:

YYY refers to the following table description, represents different packaging and special output voltage

XXXX The first X represents the last year,2020 is 0;The second X represents the month,inA-L 12 letters;The third and fourth X on behalf of the date,01-31said;

Marking	Model	VOUT Voltage	PACKAGE
31-20	DP31331-20AST	2.0V	SOT23-3
31-24	DP31331-24AST	2.4V	SOT23-3
31-28	DP31331-28AST	2.8V	SOT23-3
31-30	DP31331-30AST	3.0V	SOT23-3
31-33	DP31331-33AST	3.3V	SOT23-3
31-40	DP31331-40AST	4.0V	SOT23-3
31-44	DP31331-44AST	4.4V	SOT23-3
31-50	DP31331-50AST	5.0V	SOT23-3
31A-20	DP31331-20BST	2.0V	SOT89-3A

31A-24	DP31331-24BST	2.4V	SOT89-3A
31A-28	DP31331-28BST	2.8V	SOT89-3A
31A-30	DP31331-30BST	3.0V	SOT89-3A
31A-33	DP31331-33BST	3.3V	SOT89-3A
31A-40	DP31331-40BST	4.0V	SOT89-3A
31A-44	DP31331-44BST	4.4V	SOT89-3A
31A-50	DP31331-50BST	5.0V	SOT89-3A
31B-20	DP31331-20CST	2.0V	SOT89-3B
31B-24	DP31331-24CST	2.4V	SOT89-3B
31B-28	DP31331-28CST	2.8V	SOT89-3B
31B-30	DP31331-30CST	3.0V	SOT89-3B
31B-33	DP31331-33CST	3.3V	SOT89-3B
31B-40	DP31331-40CST	4.0V	SOT89-3B
31B-44	DP31331-44CST	4.4V	SOT89-3B
31B-50	DP31331-50CST	5.0V	SOT89-3B

Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)(1)

PARAMETER		Min	Max	Unit
VIN Voltage(1)		-0.3	32	V
EN Voltage		-0.3	32	V
VOUT Voltage(2)		2.0	5	V
Output Current		-	250	mA
Power Dissipation	SOT89-3A	-	500	mW
	SOT89-3B	-	500	mW
	SOT23-3	-	200	mW
Operating free air temperature range		-40	85	℃
Operating junction temperature,TJ		-40	150	℃
Storage temperature, Tstg		-65	150	℃
Lead Temperature（Soldering，10sec.)		-	260	℃

Note:(1)Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute – maximum – rated conditions for extended periods may affect device reliability.

（2）All voltage values are with respect to network ground terminal

Recommended Operating Conditions

PARAMETER	Min	Max	Unit
VIN Voltage(V_{IN})	4.5	30	V
VOUT Voltage(VOUT)	2	5	V
Output current(IOUT)	-	250	mA
TJ	-40	125	℃

Note : (1)All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

➢ ESD Ratings

PARAMETER	Description	Value	Unit
HBM	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
CDM	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	V

Note : (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

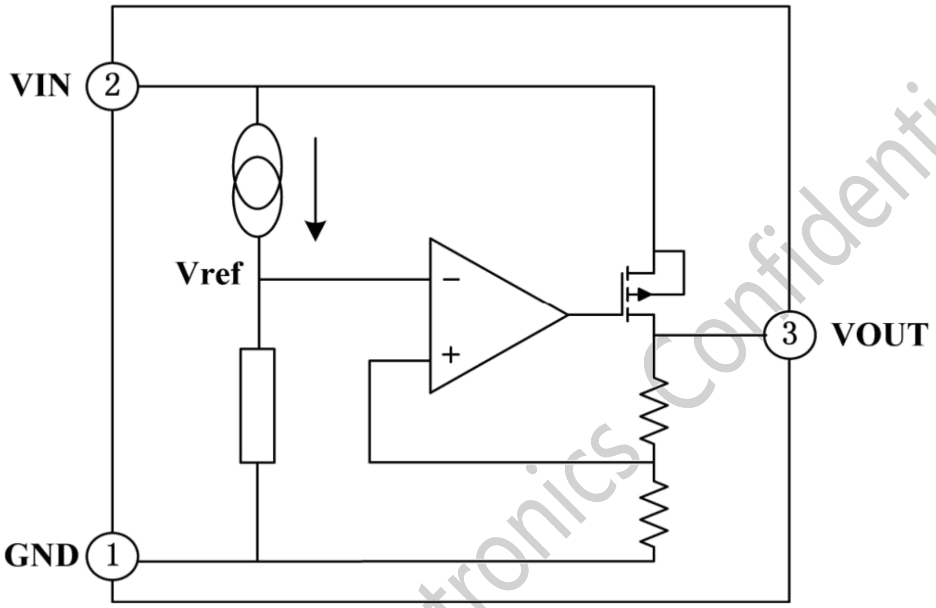
➢ Thermal Information

THERMAL METRIC	Description	SOT89-3A	SOT89-3B	SOT23-3	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)(2)	55	55	208	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88	88	112	℃/W
$R_{\theta JB}$	Junction-to-board(Bottom) thermal resistance	9.6	9.6	56	℃/W
ψ_{JT}	Junction-to-top characterization parameter	6.2	6.2	9.2	℃/W
ψ_{JB}	Junction-to-board characterization parameter	9.7	9.7	52	℃/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

BLOCK DIAGRAM



Future 1 Functional Block Diagram

ELECTRICAL CHARACTERISTICS

V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF，T_A=25℃,unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}	-	4.5	-	30	V
Output Voltage	V_{OUT}	I_{OUT}=1mA	VOUT* 0.99	-	VOUT* 1.01	V
Supply Current	I_Q	I_{OUT}=0mA		2		uA
Output Current	I_{OUT}	-		250		mA
Dropout Voltage	V_{DROP}	Iout=60mA Vout=5V		250		mV
		Iout=100mA Vout=5V		450		mV
Load Regulation	ΔV_{OUT}	V_{IN}= V_{OUT} +1V, 1mA≤I_{OUT}≤100mA		10		mV
Line Regulation	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$	I_{OUT} =10mA V_{OUT} +1V≤V_{IN}≤18V		0.01	0.2	%/V
Output Voltage Temperature Characteristics	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta T_A}$	I_{OUT} =10mA -40≤T≤+85℃		50		ppm
Output Current Limit	I_{LIM}	V_{OUT}= 0.5 x $V_{OUT(Normal)}$， V_{IN} = 5V		500		mA
Short Current	Ishort	V_{OUT}=0V		60		mA
Power Supply Rejection Rate	PSRR	F=100HZ Iout=50mA		65		dB
		F=1KHZ Iout=50mA		60		
		F=10KHZ Iout=50mA		50		
		F=100KHZ Iout=50mA		45		
Over-Temperature Protection	T_{SD}			160		℃
Over-Temperature Protection hysteresis	ΔT_{SD}			20		℃

TYPICAL CHARACTERISTICS

TJ = +25℃, VIN = (VOUT(NOM) + 1V) (whichever is greater), VEN = VIN, CIN = COUT = 1μF, unless otherwise noted.

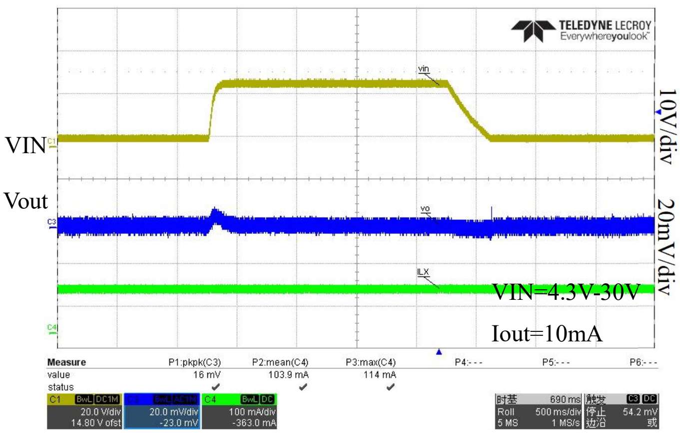


Figure1 Vout=3.3V Line Transient Response

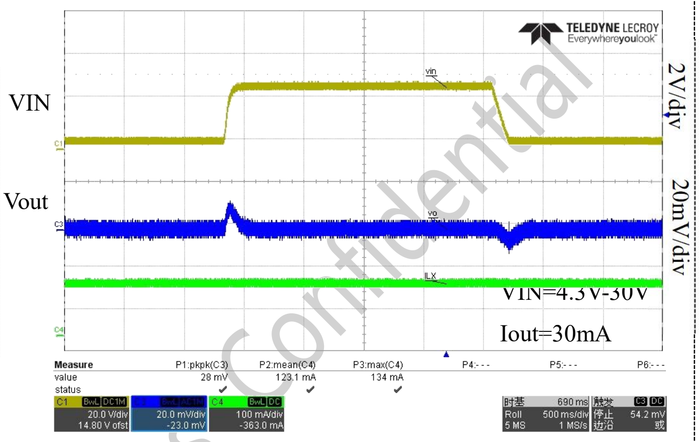


Figure2 VOUT=3.3V Line Transient Response

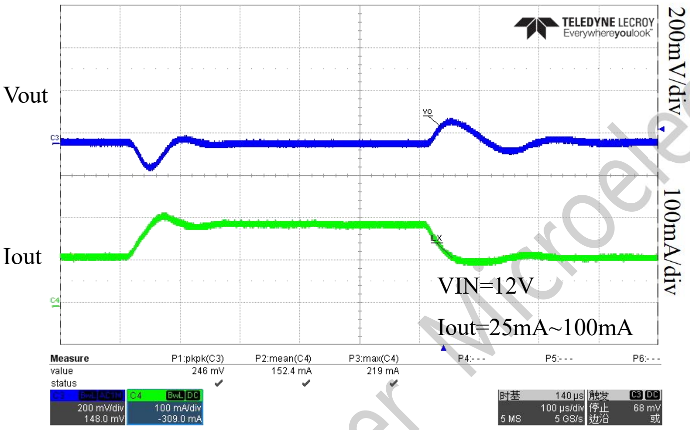


Figure3 Load Transient Response Vout=3.3V

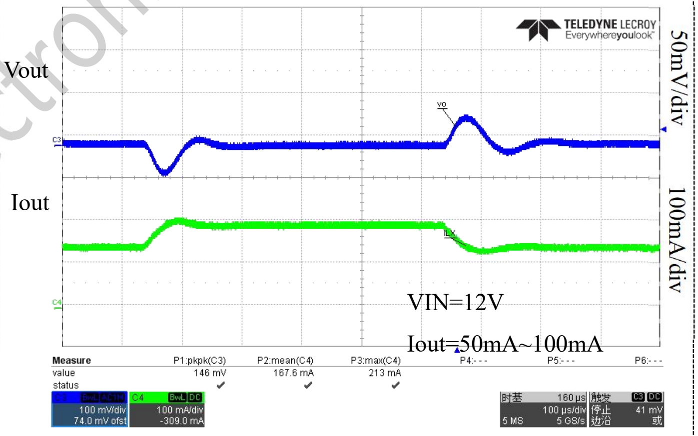
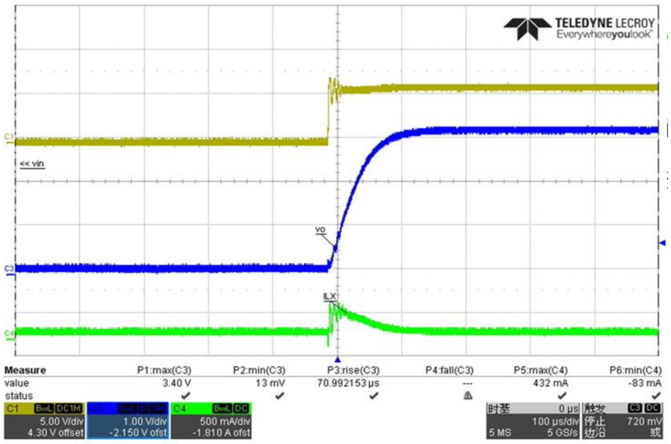


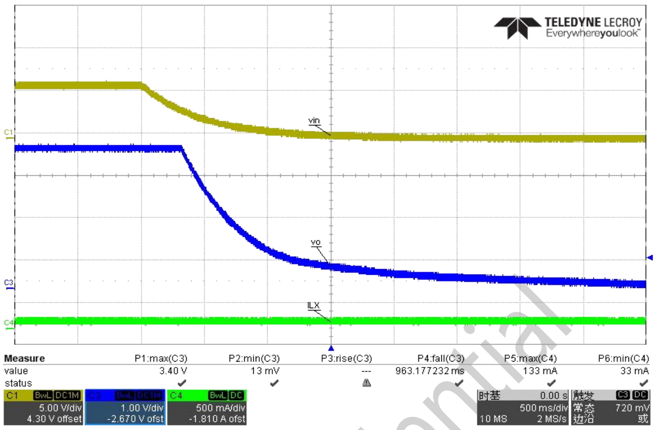
Figure4 Load Transient Response Vout=3.3V



Measure	P1:max(C3)	P2:min(C3)	P3:rise(C3)	P4:fall(C3)	P5:max(C4)	P6:min(C4)
value	3.40 V	13 mV	70.992153 µs	---	432 mA	-83 mA
status	✓	✓	✓	⚠	✓	✓

C1 BwL DC1M 5.00 V/div 4.30 V offset
C3 BwL DC1M 1.00 V/div -2.150 V ofst
C4 BwL DC 500 mA/div -1.810 A ofst
时基 0 µs 100 µs/div 5 MS 5 GS/s
触发 C3 DC 停止 720 mV 边沿 或

Figure5 Power up waveform



Measure	P1:max(C3)	P2:min(C3)	P3:rise(C3)	P4:fall(C3)	P5:max(C4)	P6:min(C4)
value	3.40 V	13 mV	---	963.177232 ms	133 mA	33 mA
status	✓	✓	⚠	✓	✓	✓

C1 BwL DC1M 5.00 V/div 4.30 V offset
C3 BwL DC1M 1.00 V/div -2.670 V ofst
C4 BwL DC 500 mA/div -1.810 A ofst
时基 0.00 s 500 ms/div 10 MS 2 MS/s
触发 C3 DC 常态 720 mV 边沿 或

Figure56 Power OFF waveform

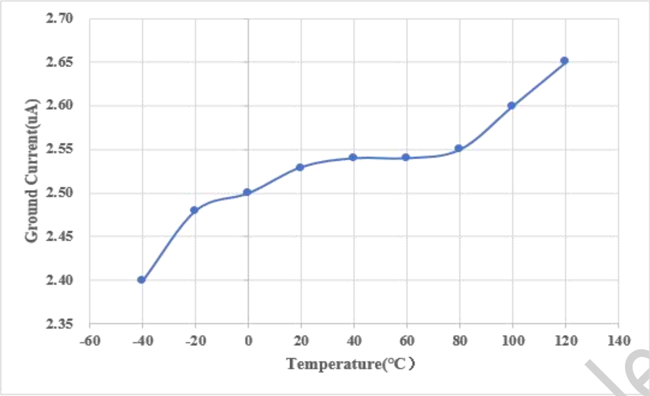


Figure7 Ground Current vs. Temperature

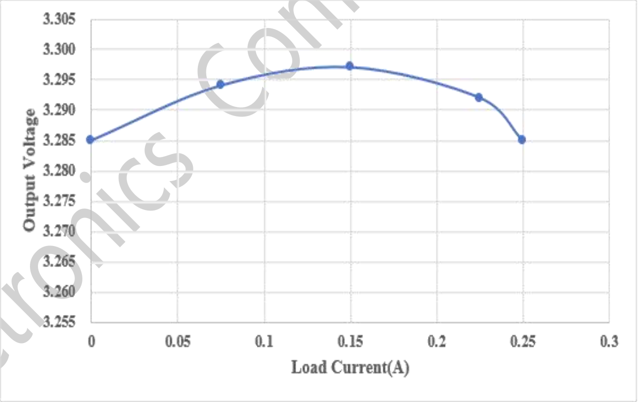


Figure8 Output Voltage vs Output Current

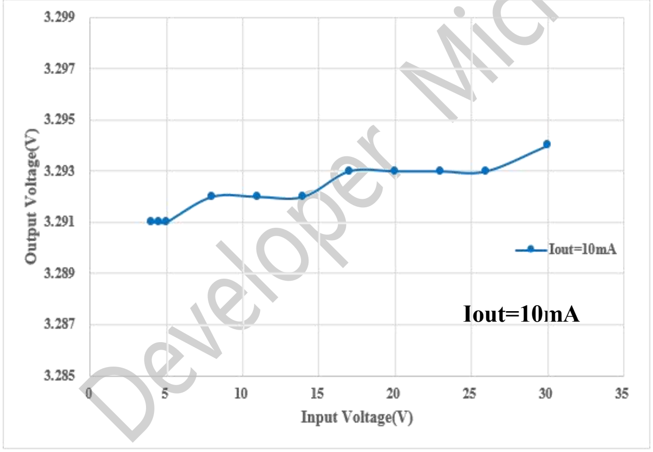


Figure9 Output Voltage vs Input Voltage

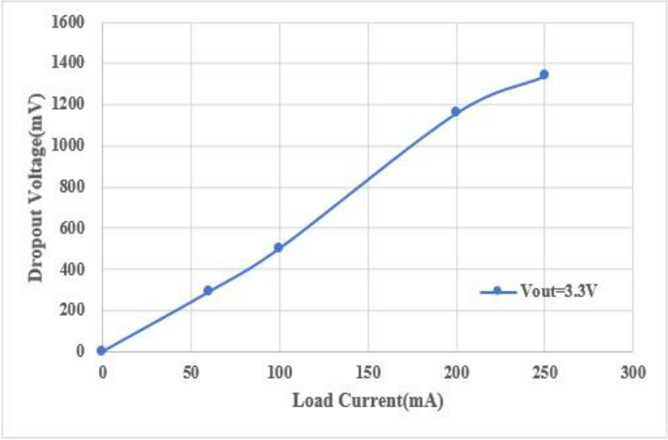


Figure10 Dropout Voltage vs Load Current

Functions Description

- **Feature Description**

The DP31331 series are a group of positive voltage regulators manufactured by CMOS technologies with high ripple rejection, ultra-low noise, low power consumption and low dropout voltage, which can prolong battery life in portable electronics.

The DP31331 series work with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications.

The DP31331 series consume less than 0.1μA in shutdown mode and have fast turn-on time less than 50μS.The series are very suitable for the battery-powered equipment,

- **Thermal Shutdown**

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160 ° C typically. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

- **Output Current Limit and Short-Circuit Protection**

When overload events happen, the output current is internally limited to 500mA (TYP). When the OUT pin is shorted to ground, the short-circuit protection will limit the output current to 100mA (TYP).

APPLICATION INFORMATION

The DP31331 is a low VIN, ultra-low noise and low dropout LDO and provides 500mA output current.

These features make the device a reliable solution to solve many challenging problems in the generation of clean and accurate power supply.

The high performance also makes the DP31331 useful in a variety of applications. The DP31331 provides the protection functions for output overload, output short-circuit condition and overheating.

The DP31331 provides an EN pin as an external chip enable control to enable/disable the device. When the regulator is in shutdown state, the shutdown current consumes as low as 0.03μA (TYP).

- **Input capacitors selection**

The input decoupling capacitor should be placed as close as possible to the IN pin to ensure the device stability. 1μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance. When VIN is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings.

- **Output capacitors selection**

The output capacitor should be placed as close as possible to the OUT pin. 1μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance. The minimum effective capacitance of COUT that DP31331 can remain stable is 1μF. For ceramic capacitor, temperature, DC bias and package size will change the effective capacitance, so enough margin of COUT must be considered in design. Additionally, COUT with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

- **PCB Layout**

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance

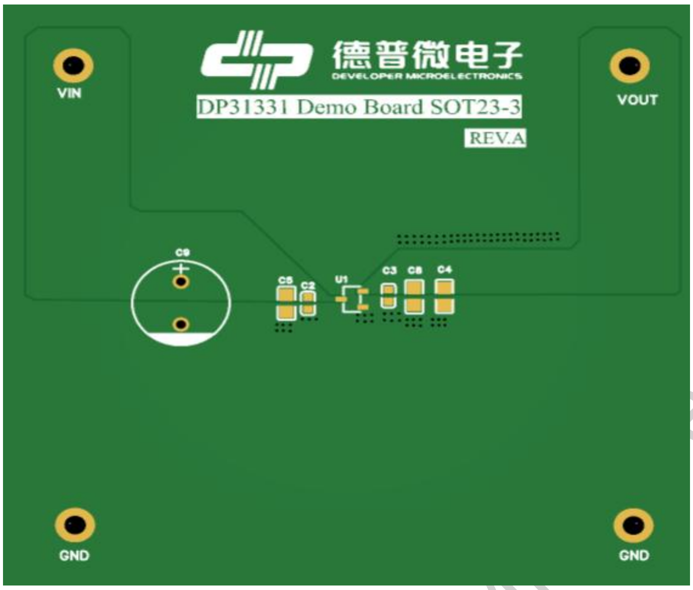
1. The input bypass capacitor C5 and C2 must be placed as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VIN pin to reduce the high frequency injection current.

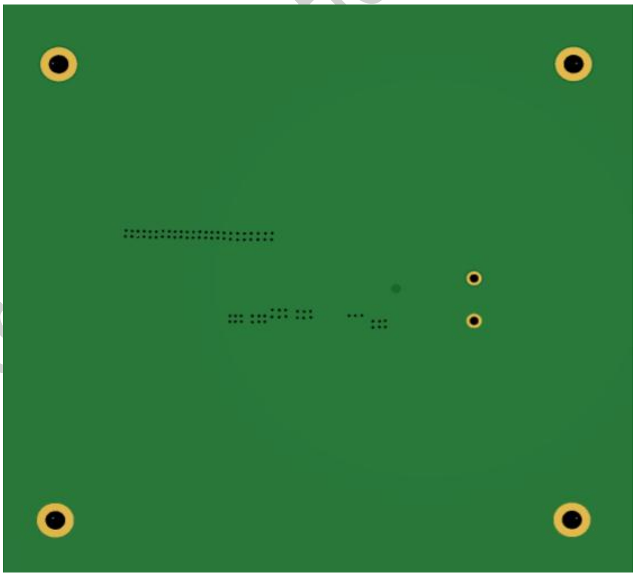
2. The output capacitor, COUT should be placed close to the junction of Vout Pin.

3. The ground connection for C3, C4, C8 and C5, C2 should be as small as possible and connect to system ground plane at only one spot (preferably at the COUT ground point) to minimize injecting noise into system ground plane.

4. Large GND Copper Pour near IC is recommended to minimize the heat of IC.

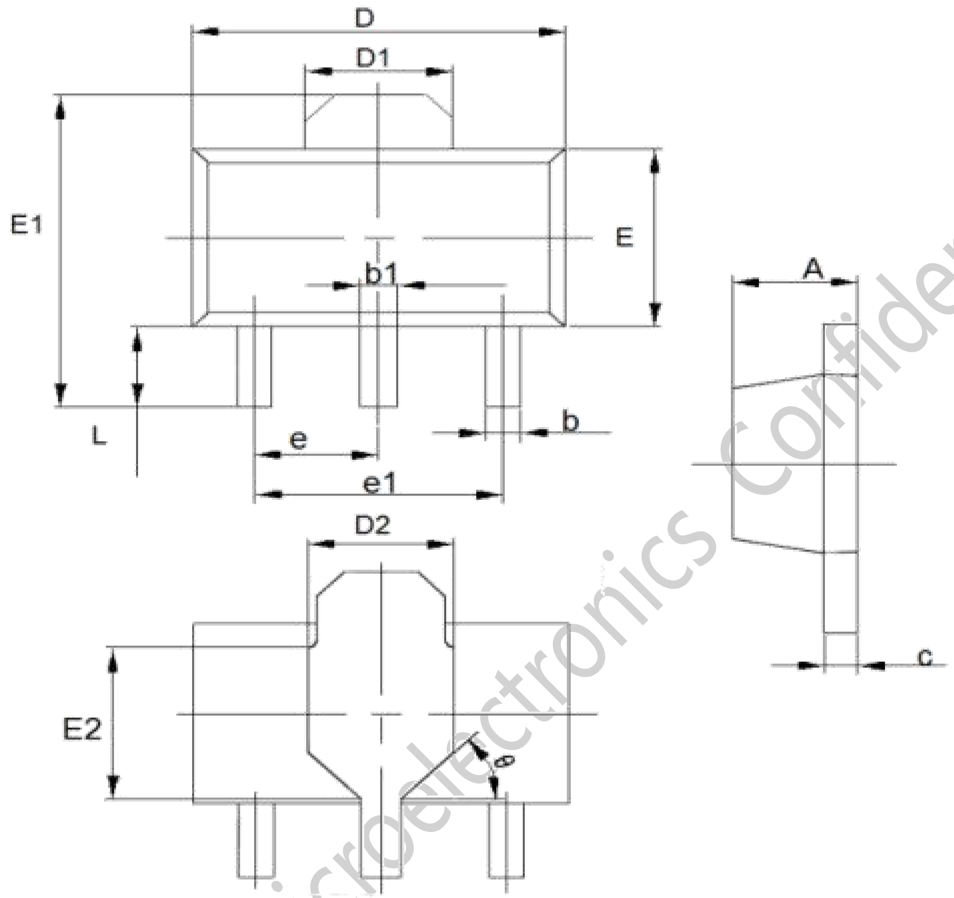
- **Layout Example:**





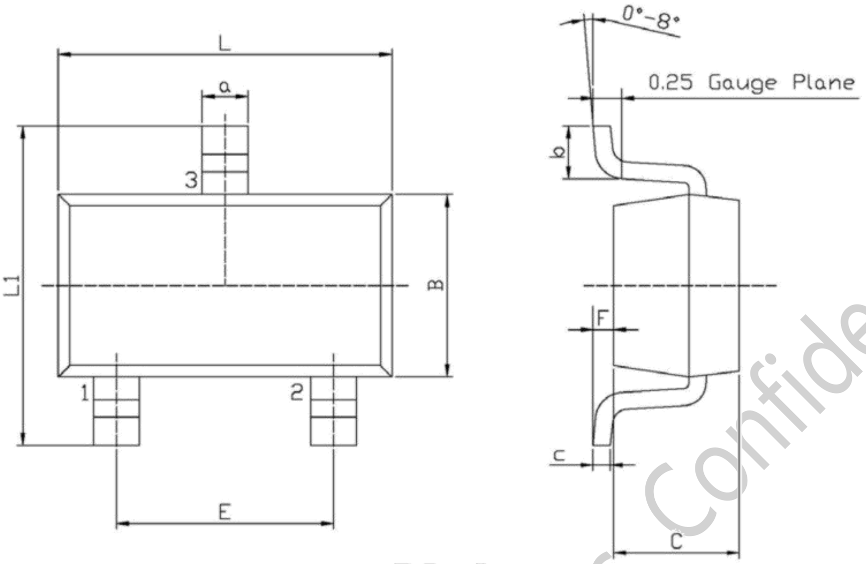
PACKAGE DIMENSION

SOT89-3



Symbol	Dimensions in Millimeters		Symbol	Dimensions in Millimeters	
	Min	Max		Min	Max
A	1.4	1.6	E1	3.94	4.4
b	0.32	0.52	E2	1.9(TYP)	
b1	0.4	0.58	e	1.5(TYP)	
c	0.35	0.45	L	0.8	1.2
D	4.4	4.6	θ	45°	
D1	1.55(TYP)				
D2	1.75(TYP)				
e1	3.0(TYP)				
E	2.3	2.6			

SOT23-3



Symbol	Dimensions in Millimeters	
	Min	Max
L	2.82	3.02
B	1.50	1.70
C	0.90	1.30
L1	2.60	3.00
E	1.80	2.00
a	0.35	0.50
c	0.10	0.20
b	0.30	0.55
F	0	0.15

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