DP3254 16 Channel 32 scans Low-turning PWM Constant Current Driver

1 Overview

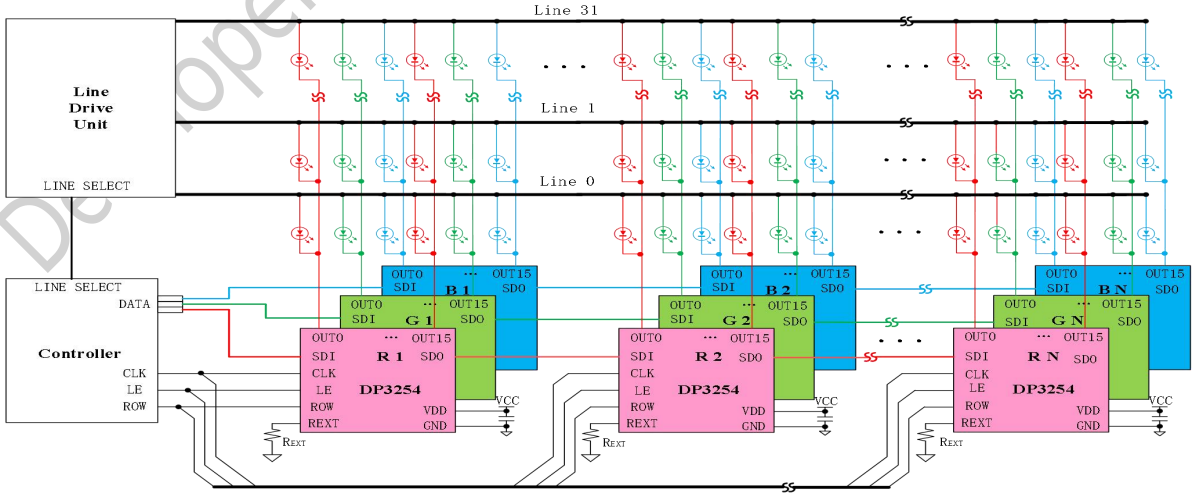
DP3254 Is a 16-channel low-transition PWM constant current drive chip designed for LED display. The high-precision current generating circuit technology is integrated, the current error between the chips can be controlled within 2.0%, and the low gray high brush mode is added to improve the low gray refresh rate. And integrated with a variety of exclusive technology to improve the display effect of the LED display, which can bring more improvements to the display screen.。

2 Features

- Power supply voltage range: 2.6~5.5V
- Operating temperature range: -40℃ ~85℃
- Scan range: 1~32 scan, any adjustable
- 16 constant current output channels
- Support for no external resistance mode
- Constant flow output range
  - 0.5mA～18mA (V_{out}=0.3V)
  - 0.5mA～25mA (V_{out}=0.45V)
- Inter-channel current error
  - Typical value: ± 1.2% Maximum value: ± 2.5% (V_{out}=0.45V)
- Inter-chip current error
  - Typical value: ± 1.5% Maximum value: ± 2.0%
- High gray independent refresh, no black field between frames
- Low gray and high brush: low gray supports 1~8 times display frame rate
- The imum refresh rate supports 128 times frame rate (7680Hz)
- Optimize the display status
  - Improve the low-gray uniformity
  - Improve the first line of partial darkness phenomenon
  - Improve the phenomenon of the ghost shadows
  - Improve the high and low grey coupling
  - Improve cross-plate coupling
- Integrated PLL produces in-house GCLK with a lower EMI
- Packaging form: QSOP24 / QFN 24
- Excellent ESD features

3 Application Fields

- High refresh rate LED video display
- One color two color full color LED display
- High-density small-spacing LED light board display



DP3254 A Schematic diagram of the typical application

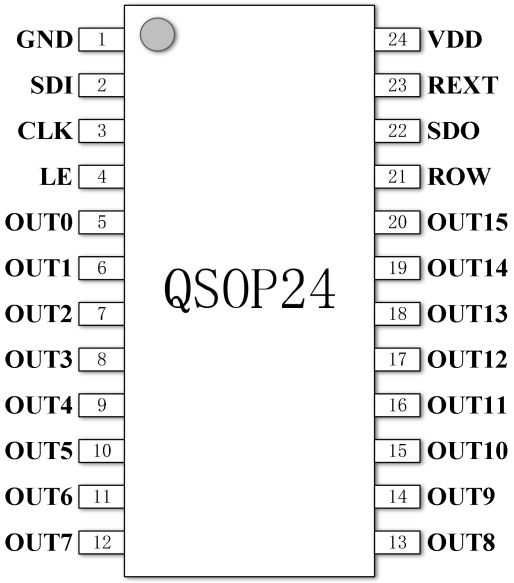
catalogue

Revise the history

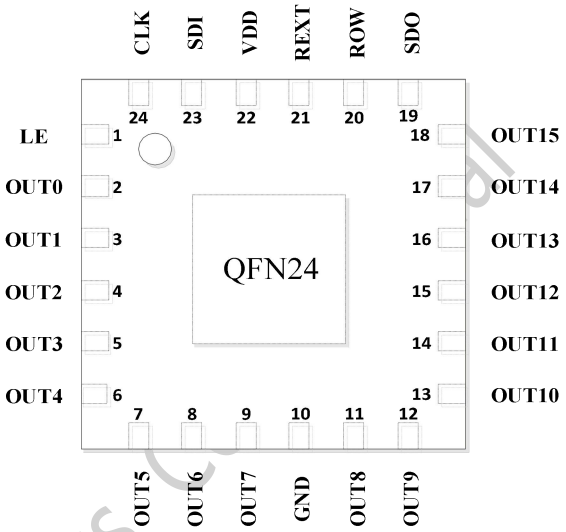
edition	Revised date	Revised	Revised content
V 0.1	2023.07	Wang Mei	The initial version
V0.2	2023.08	Wang Mei	Modify the instructions and the registers
V0.3	2023.11	Wang Mei	Modify the QFN encapsulation pin definitions

4 Product Description

- The pin definition



QSOP24 Pin definition diagram



The QFN 24 pin definition diagram

- Feet instructions

QSOP24 Pin number	The QFN 24 pin number	Feet name	Feet instructions
1	10	GND	Chip ground end
2	23	SDI	Serial data input side
3	24	CLK	Serial clock input end
4	1	LE	The latch end of the data and instructions, and different LE lengths represent different instructions
5 ~ 20	2 ~ 9 11 ~ 18	OUT0 ~ OUT15	Constant flow output
21	20	ROW	Change the line signal
22	19	SDO	Serial data output side
23	21	REXT	Connect external resistance
24	22	VDD	Chip power end

- Product order information

product name	Packaging form	manner of packing	Quantity / plate	Wet sensitivity level
DP3254	QSOP24	braid	4000	MSL=3
	QFN24	braid	5000	

- Product marking

QSOP24

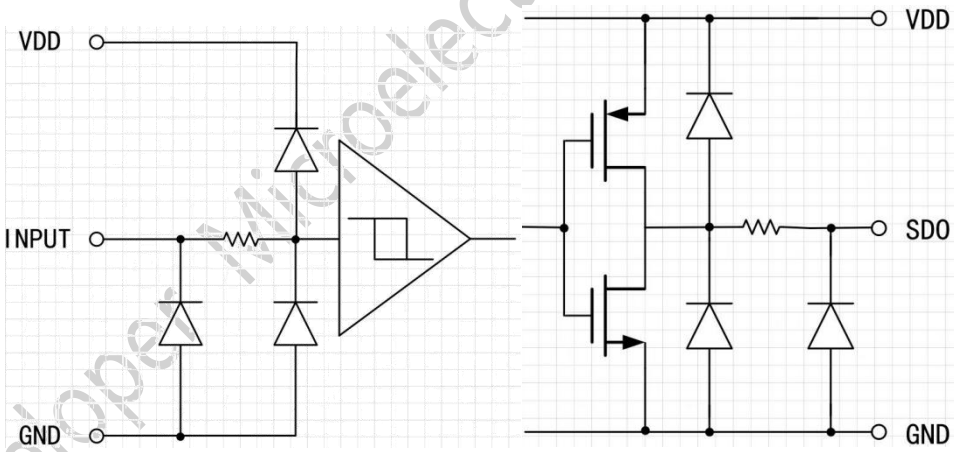
QFN24

DP3254 The name of the product
XXXXXX Represents the product lot number

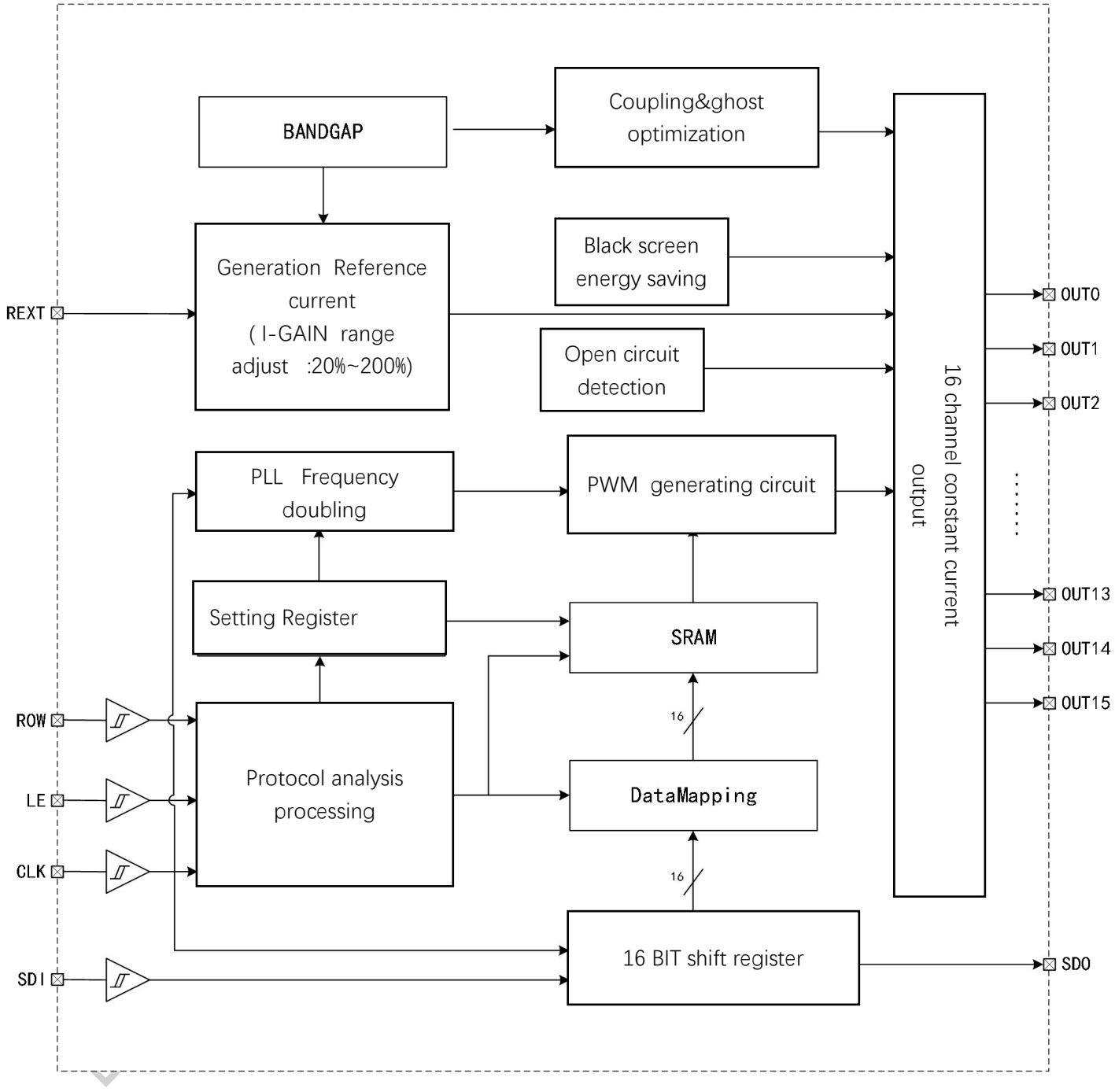
5 Circuit Schematic Diagram

5.1 Input-output equivalent circuit

SDI, CLK, LE, OE input end SDO output end



5.2 Internal Circuit Block Diagram



A Schematic diagram of the internal circuit

6 Parameter List

6.1 Maximum Limit Parameter

project	symbol	rating	unit
supply voltage	V_{DD}	0 ~ 5.5	V
output	I_O	25	mA
input voltage	V_{IN}	-0.4 ~ V_{DD}+0.4	V
Output tolerance voltage	V_{OUT}	11	V
clock frequency	F_{CLK}	25	MHz
working temperature	T_{opr}	-	-
Storage temperature	T_{stg}	-55 ~ 150	℃

- All the voltage values are based on the chip ground end (GND) as the reference point, and the test temperature of the maximum limit parameter is 25℃.
- The actual working conditions exceeding the specified value may cause permanent damage to the components; the actual working conditions falling slightly below the maximum value and working for long hours may reduce the reliability of the components. The above is only partially specified values, and this product does not support functional operation under other conditions than the specification.
- The highest welding temperature of the table paste product shall not exceed 260℃. The temperature curve shall be set by the factory according to the J-STD-020 standard, refer to the actual factory and the manufacturer of the tin paste.

6.2 ESD Grade

6.2.1 Contact ESD

symbol	condition		least value	representative value	crest value	unit
$V_{(ESD)}$	Human Discharge Model (HBM)[1]	OUTn Pin-GND	-	-	-	kV
		OTHER Pin-GND	-	-	-	kV
	machine model (MM)[2]	OUTn Pin-GND	-	-	-	kV
		OTHER Pin-GND	-	-	-	kV

- [1] The lowest HBM model ESD voltage of all the pins meets the Class-3B standard in the JEDEC JS-001-2017 file.
- [2] The lowest MM model ESD voltage of all pins meets the Class-C standard for the JEDEC EIA / JESD22-A115C file.

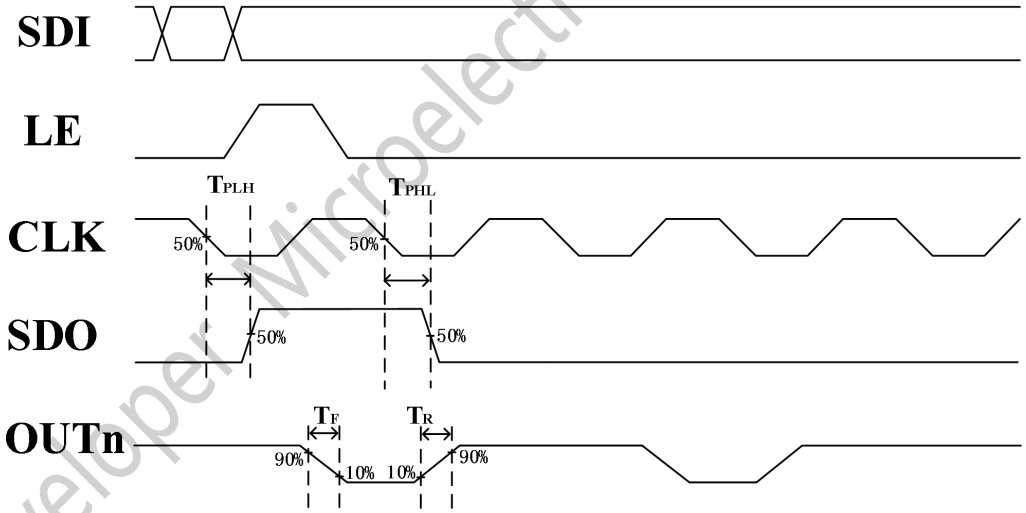
6.3 Electrical Characteristics (VDD=3.5V~5V, Ta=25℃)

project		symbol	test circuit	test condition		least value	representative value	crest value	unit
REXT voltage characteristic		VR_TT	1	V_{DD}=5V,R_{EXT}=1K IGAIN=100%,T_a=25℃		-	1.533	-	V
		VR_LT		V_{DD}=5V R_{EXT}=1K IGAIN=100%	T_a=-40℃	-	1.56	-	V
		VR_HT			T_a=85℃	-	1.495	-	V
		VR_LV		T_a=25℃ R_{EXT}=1K IGAIN=100%	V_{DD}=5.5V	-	1.535	-	V
		VR_HV			V_{DD}=2.6V	-	1.521	-	V
Constant flow output inflection point		V_{OUT1}	2	V_{DD}=5.0V R_{EXT}=1k Turning point level 0	IOUT=18mA	-	350	-	mV
		V_{OUT2}			IOUT=9mA	-	290	-	mV
		V_{OUT3}			IOUT=4.5mA	-	260	-	mV
		V_{OUT4}		V_{DD}=5.0V R_{EXT}=1k Turning point level 1	IOUT=18mA	-	460	-	mV
		V_{OUT5}			IOUT=9mA	-	390	-	mV
		V_{OUT6}			IOUT=4.5mA	-	360	-	mV
Constant current source output range		IOUT	2	Turning point level 0		0.5	-	18	mA
		IOUT1		Turning point level 1		0.5	-	25	mA
Interchip output current error		DCHIP	2	VDS=0.6V		—	±1.5	± 2.0	%
Interchannel output current error		DCHL	2	VDS=0.6V		—	± 1.2	±2.5	%
Constant current error / VDS, the variation amount		%/Δ VDS	2	VDS=0.3~3.0V		—	—	± 1.0	%/V
Constant current error / VDD variation		%/Δ VDD	2	VDD=3.5V~5.0V		—	—	± 1.0	%/V
Output voltage at the ON		$V_{O(ON)}$	2	OUT0~OUT15		0.3	-	V_{DD}	V
SDO drive current	high level	IOH	3	VDD=5V		—	-22	—	mA
	low level	IOL				—	23	—	mA
output level	high level	VOH	4	IOH=-1mA		4.6	—	—	V

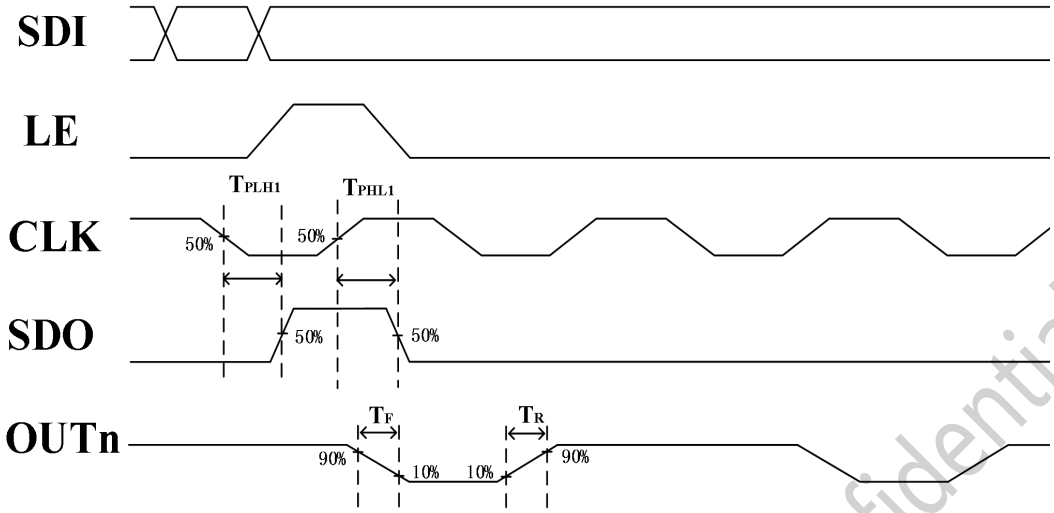
low level	VOL		IOL=1mA	—	—	0.4	V
High-level logic input voltage	V_{IH}	5	-	0.7*V_{DD}	-	V_{DD}	V
Low-level logic input voltage	V_{IL}		-	GND	-	0.3*V_{DD}	V
Power supply current (with resistance) (White screen power consumption)	I_{DD1}	6	R_{EXT}=3K, white screen IOUT = 6 mA, with a refresh rate of 3,840	-	4.69	-	mA
Power supply current (with resistance) (Black screen energy-saving power consumption)	I_{DD3}	6	R_{EXT}=3K, black screen IOUT = 6 mA, and the performance is preferred	-	2.95	-	mA
	I_{DD4}		R_{EXT}=3K, black screen IOUT = 6 mA, and the low power consumption is preferred	-	1.29	-	mA
	I_{DD5}		R_{EXT}=3K, black screen IOUT = 6 mA, with very low power consumption	-	0.68	-	mA
Power supply current (no resistance) (White screen power consumption)	I_{DD1}	6	White screen IOUT = 6 mA, with a refresh rate of 3,840	-	4.26	-	mA
Power supply current (no resistance) (Black screen energy-saving power consumption)	I_{DD3}		blank screen IOUT = 6 mA, and the performance is preferred	-	2.88	-	mA
	I_{DD4}		blank screen IOUT = 6 mA, and the low power consumption is preferred	-	1.45	-	mA
	I_{DD5}		blank screen IOUT = 6 mA, with very low power consumption	-	0.79	-	mA

6.4 Dynamic Characteristics (VDD=3.5V~5V, Ta=25℃)

project	symbol	test circuit	test condition	least value	representative value	crest value	unit
The CLK-SDO delay	TPHL	7	VDD=5V, FDCLK=12.5MHz	-	15	-	ns
The CLK-SDO delay	TPLH			-	15	-	ns
The CLK-SDO delay	TPHL 1			-	25	-	ns
The CLK-SDO delay	TPLH 1			-	15	-	ns
Constant current output rise time	T R		IOUT=10mA, ΔVOUT=3V	-	65	-	ns
Constant current output drop time	T F			-	50	-	ns



Time-series waveform diagram of single along transmission sequence

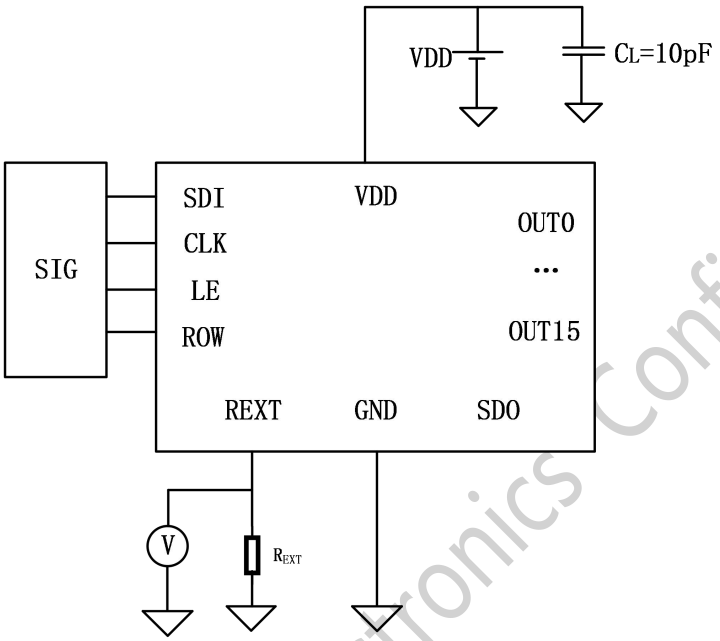


Wwaform pattern of double transmission sequence

7 Test Circuit Diagrams

7.1 Test Circuit 1

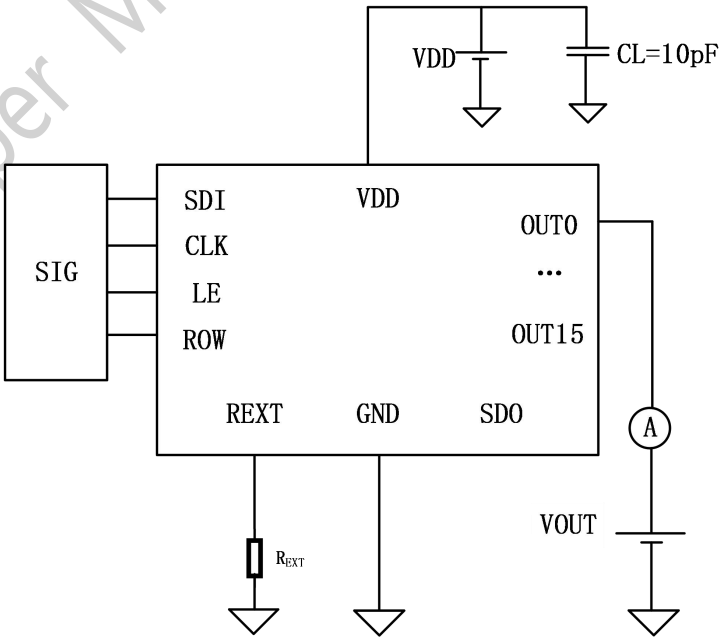
- External resistance voltage



A Schematic diagram of the test circuit 1

7.2 Test Circuit 2

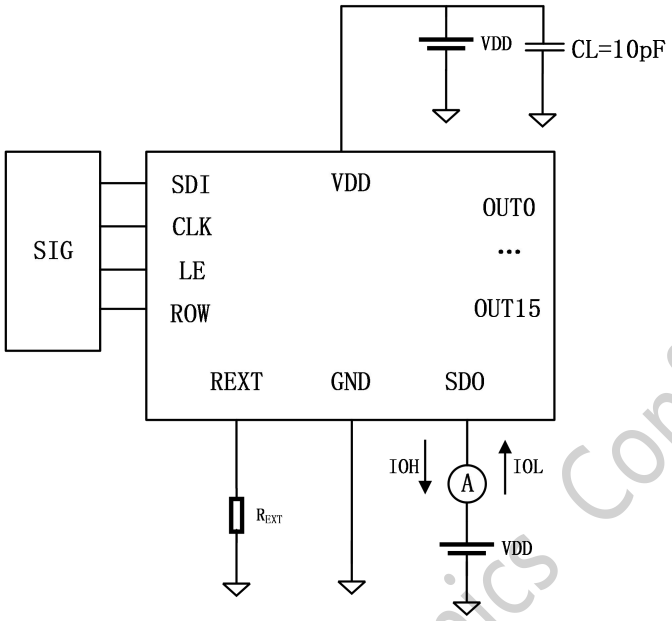
- Constant current output inflection point voltage & corresponding inflection point current (in open circuit detection state)



A Schematic diagram of the test circuit 2

7.3 Test Circuit 3

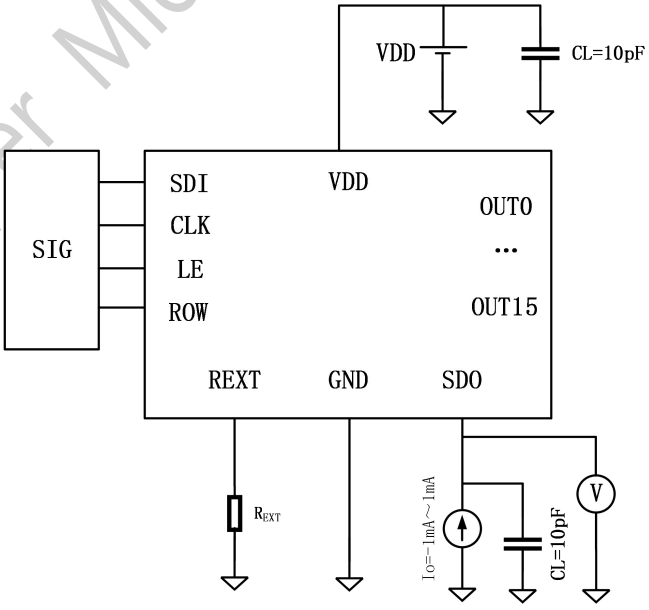
- IOH、IOL



A Schematic diagram of the test circuit 3

7.4 Test Circuit 4

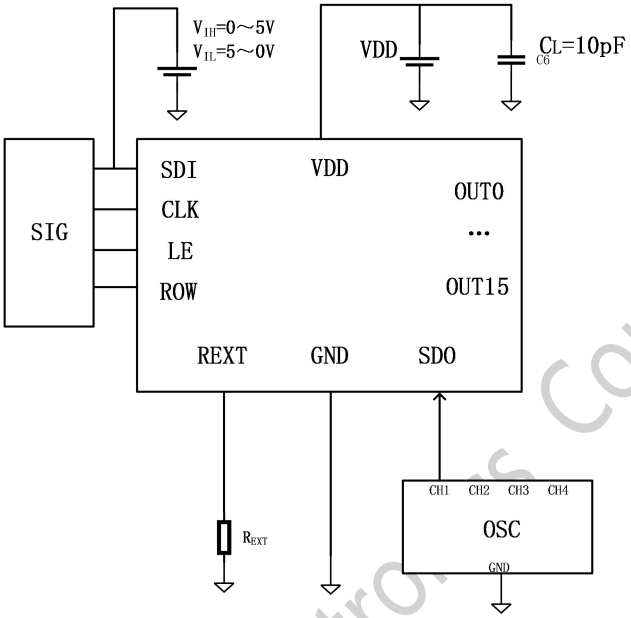
- VOH、VOL



A Schematic diagram of the test circuit 4

7.5 Test Circuit 5

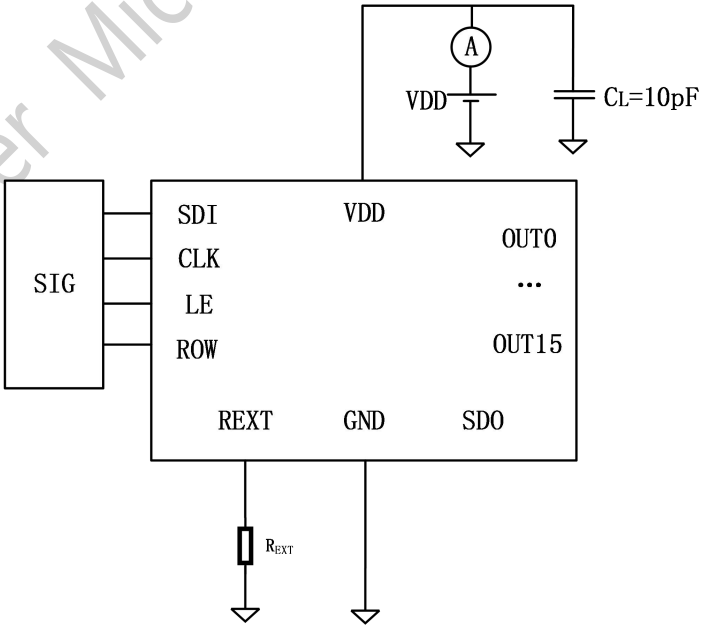
- VIH、VIL



A Schematic diagram of the test circuit 5

7.6 Test Circuit 6

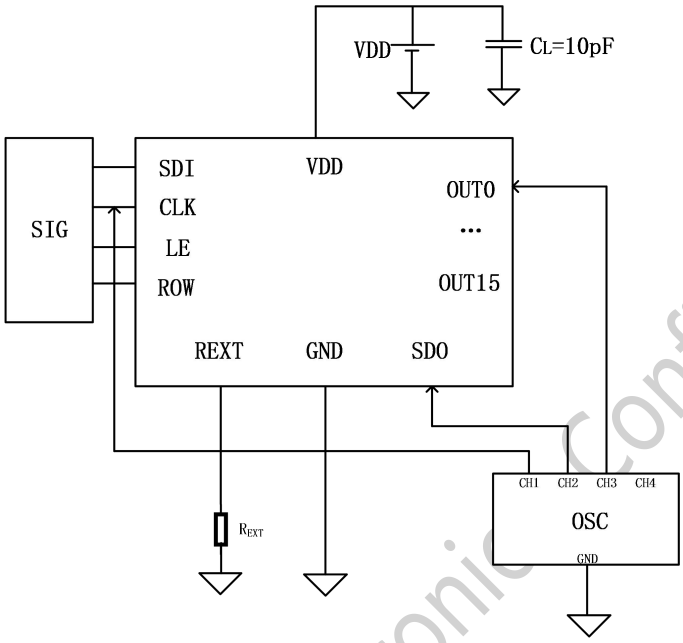
- source current



A Schematic diagram of the test circuit 6

7.7 Test Circuit 7

- dynamic characteristis



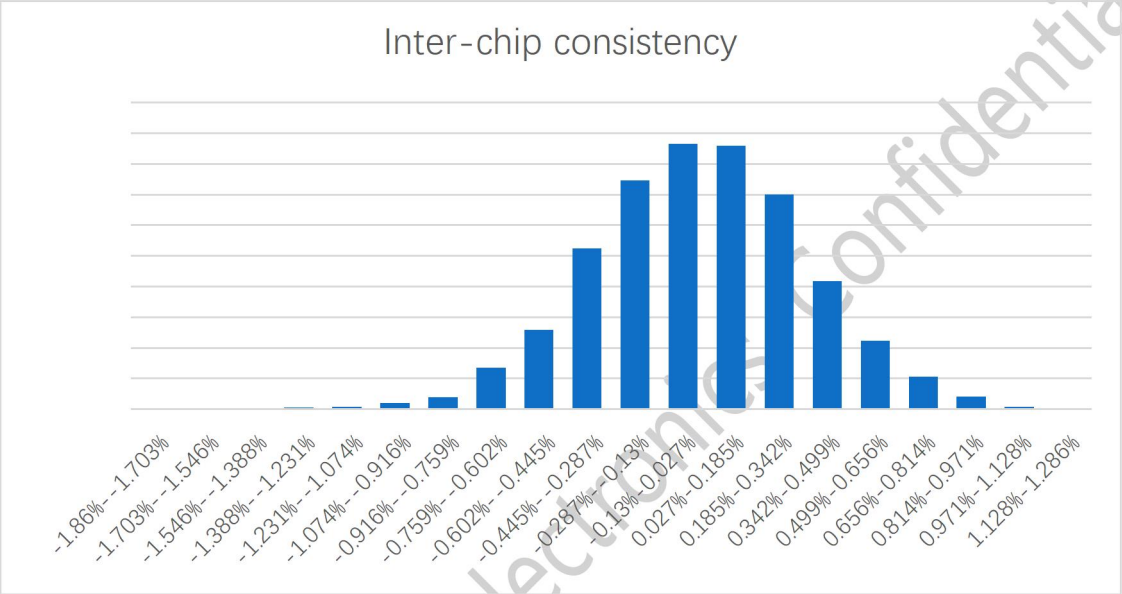
A Schematic diagram of the test circuit 7

8 Typical Feature Diagram

8.1 Constant Current Source Accuracy Test Chart

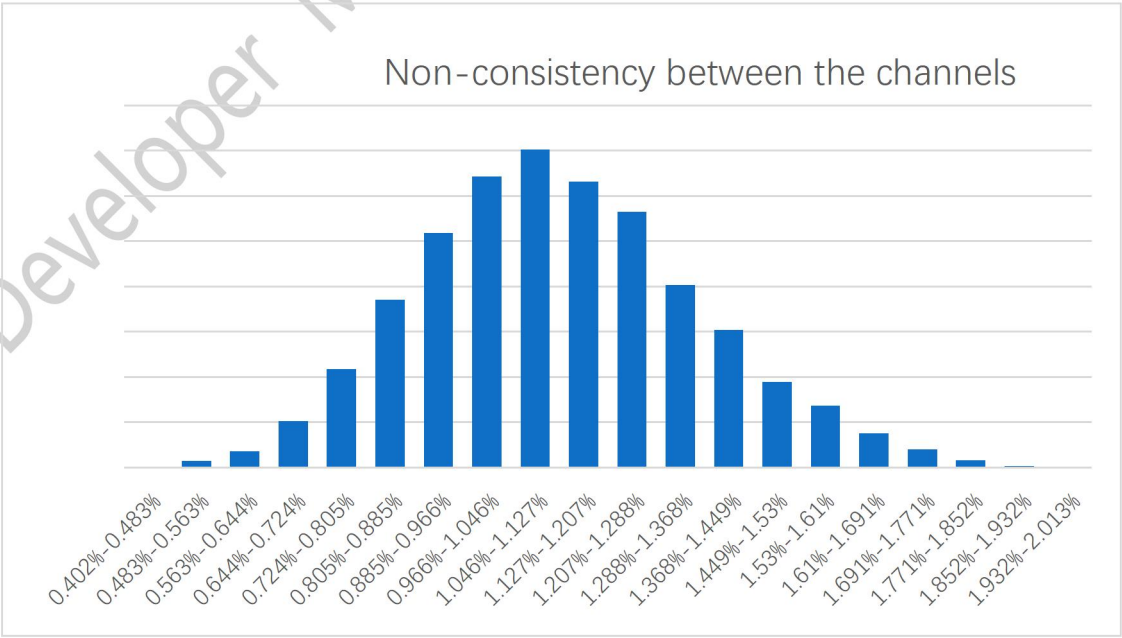
8.1.1 Inter-chip Current Error

$$\text{Interchip current error} = \frac{\text{Average value of the channel current} - \text{All chip channel average values}}{\text{All chip channel average values}}$$



8.1.2 Inter-channel Current Error

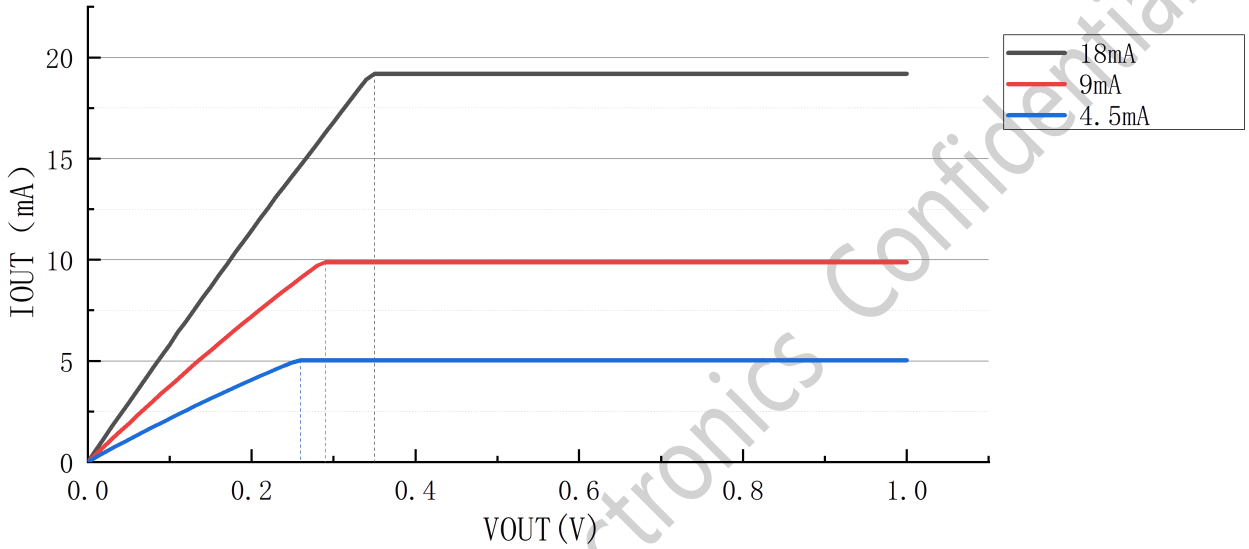
$$\text{Inter-channel current error} = \frac{Imax - Imin}{Imax + Imin}$$



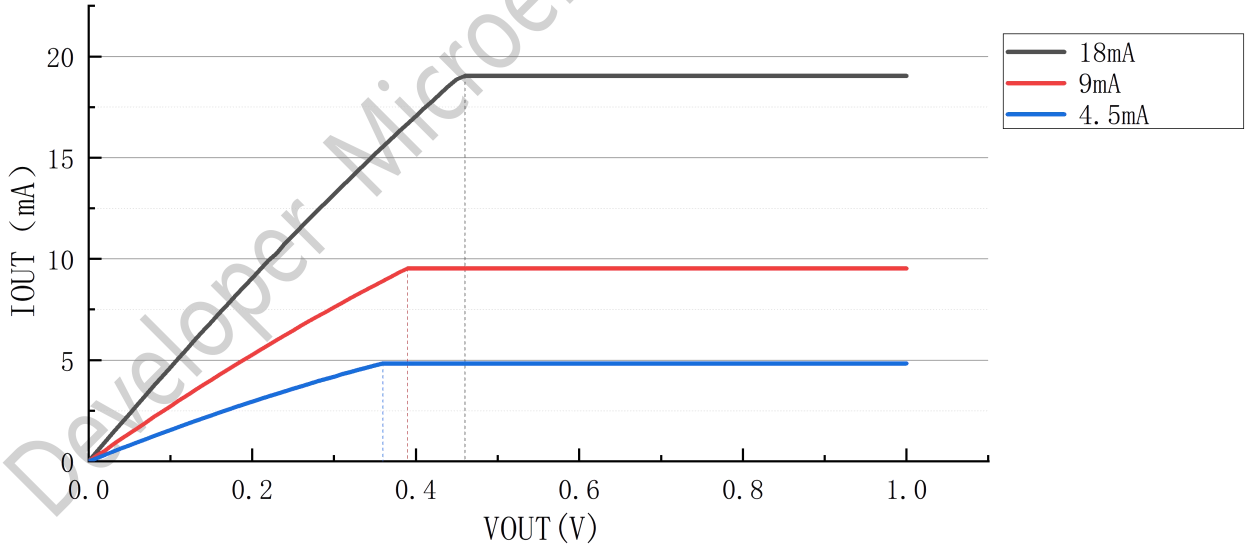
8.2 Constant Flow Source Iinflection Point

When applying DP3254 to LED display design, the current difference between channels and even between chips is minimal. This is derived from the excellent constant current output characteristics of the DP3254:

- The maximum current between the chip channels is less than ± 2.5%, while the maximum current error between the chips is less than ± 2.0%;
- When the load end voltage (V out) changes, the stability of the output current is not affected, as shown in the figure below:



Association curve between IOUT and VOUT at low turn, VDD=2.6V-5.5V



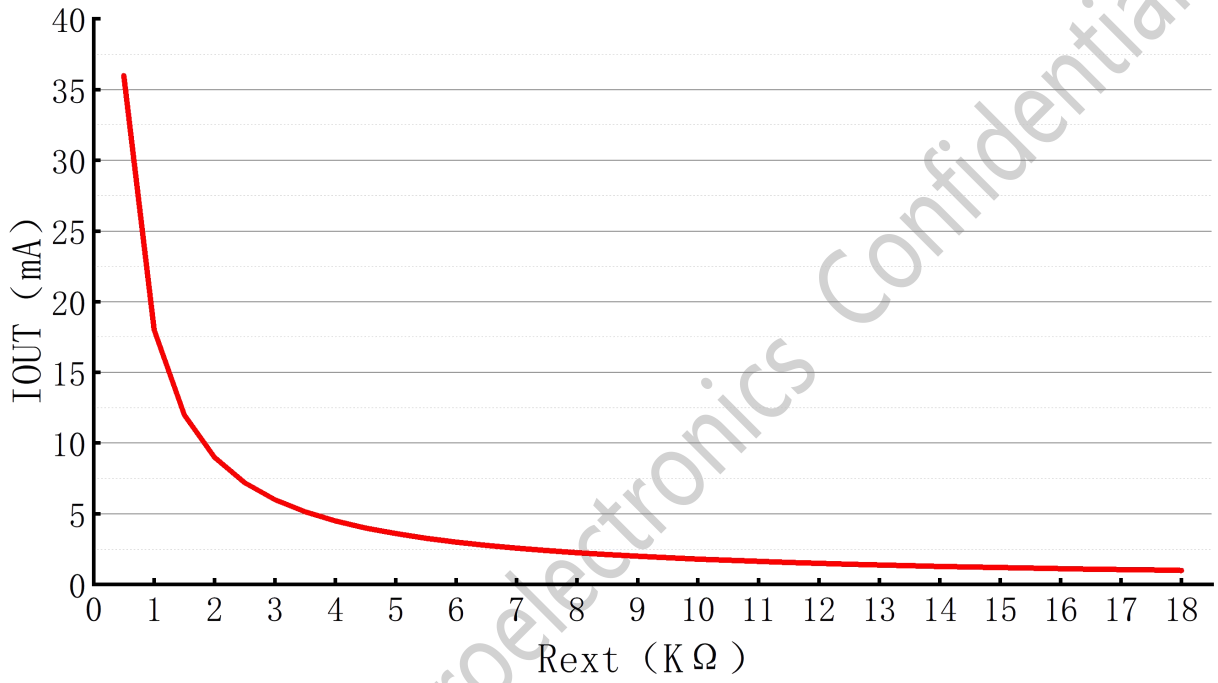
The relationship curve between IOUT and VOUT at not low turn, VDD=2.6V-5.5V

8.3 Adjust The Output Current By Using The External Resistance

The output current value is calculated as follows:

$$\mathbf{IOUT} = \frac{IGAIN*18}{Rext} \leq, \mathbf{20\%\ \ IGAIN\ \ 200\%} \leq$$

R in formula$_{EXT}$Is the ground-to-ground resistance value of the 23PIN REXT port of the chip. For example, when the current gain IGAIN = 100%, R_{EXT}At = 1 kΩ, the output current value of 18 mA can be obtained by calculating the formula.



IGAIN=100%，R_{EXT}The relationship curve with Iout

8.4 The No-resistance Mode Adjusts The Current By A Register

The output current value is calculated as follows:

Iout=[70uA+0.4uA*(reg0x0f<6:0>-16)]*reg0x08<7:0>*(1+0.5*reg0x0b<5>)

9 Typical Display Effect Pattern

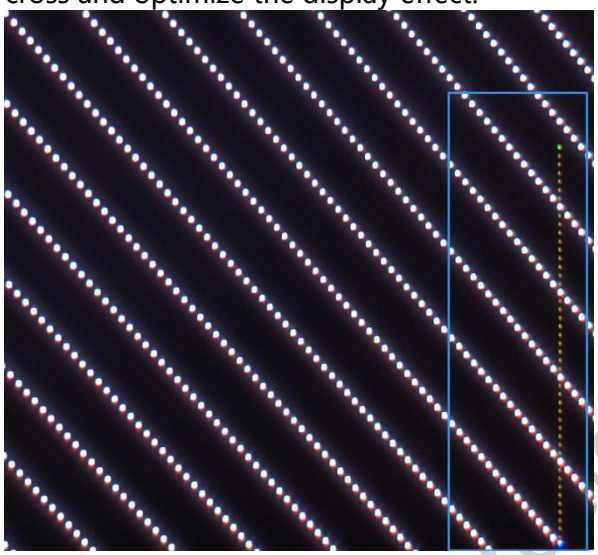
- The specific display effect will be affected by the lamp plate conditions and register parameters, and the following test results are only of reference significance.

9.1 Display Effect

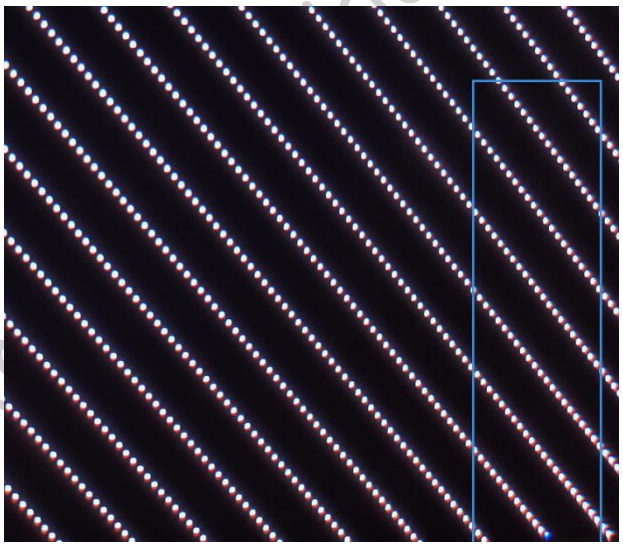
9.1.1 Remove The Open Circuit Break Point Cross

The following is a comparison of the display effect before and after removing the open circuit broken cross. You can see:

- The chip performs the function of removing the open bad point cross, which can remove the bad point cross and optimize the display effect.



Show the effect before removing the open break point cross

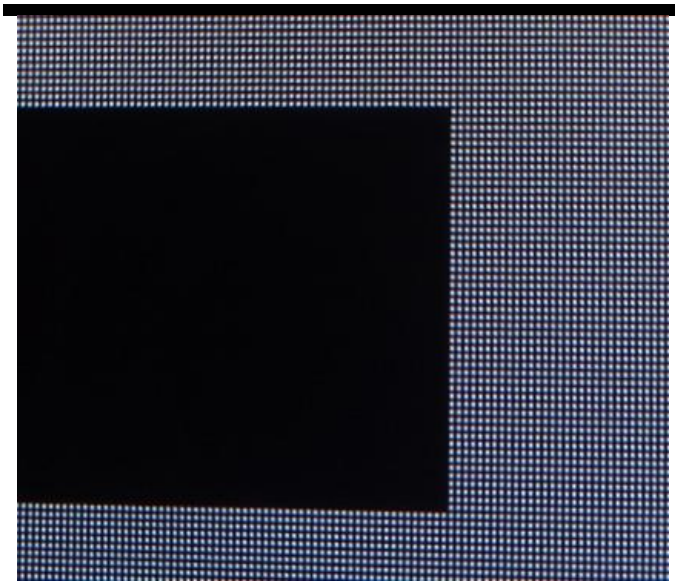


Show the effect after removing the open break point cross

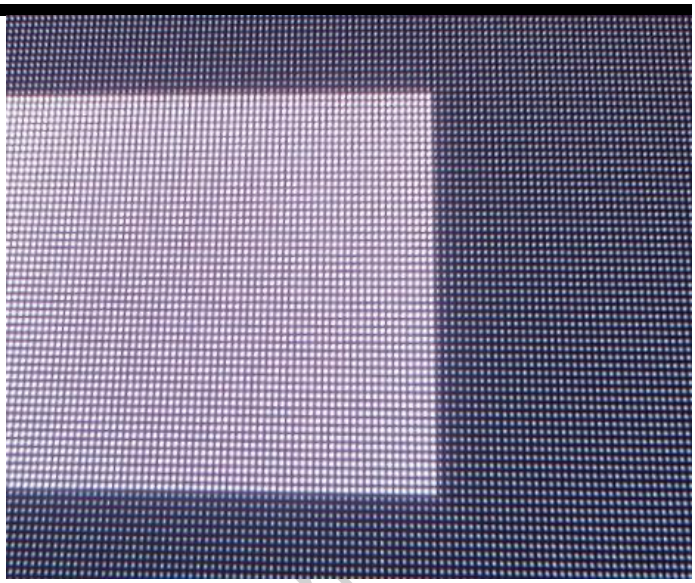
9.1.2 High and Low Gray Interference and Coupling Display Bad Effect Optimization

The following figure shows the optimization effect of high and low gray interference and coupling display. It can be seen that:

- Neither the low gray coupling between black block and white block can be felt.
- The chip showed a good display effect.



Black block low-grey coupling test shows the effect

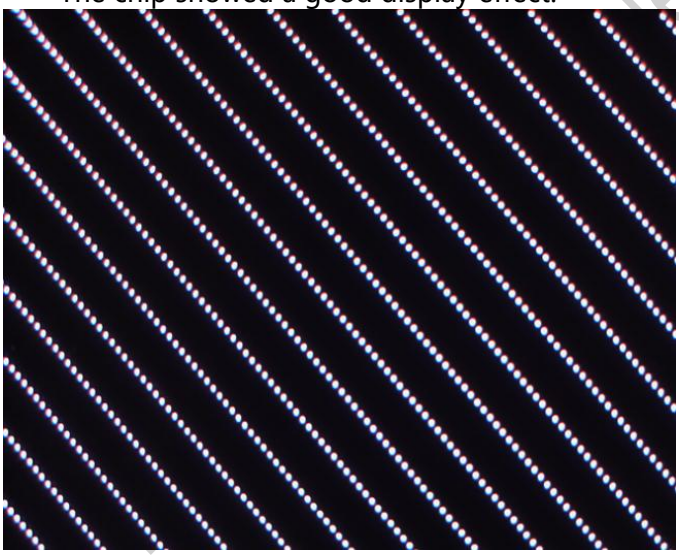


The white block low gray coupling test showed the effect

9.1.3 Remove Ghostiness and Bandless Lighting Effects

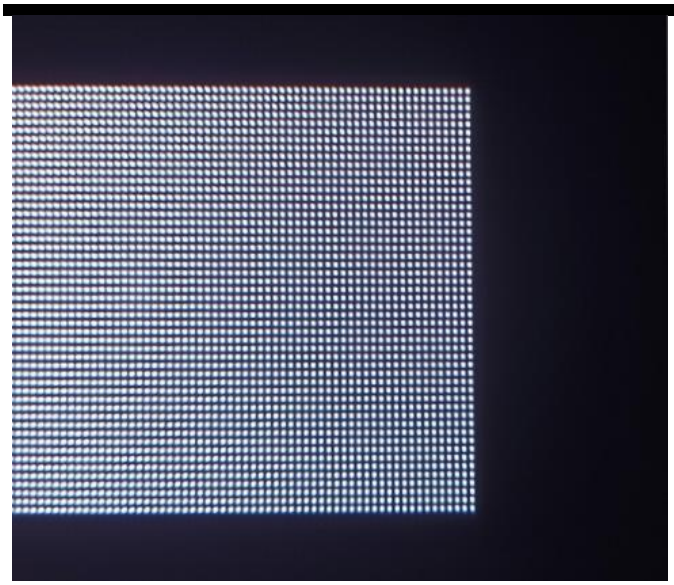
Below is the removal of ghosting and bandless lighting effect that can be seen:

- Inclined scanning under the ghost, text ghost and other problems can not be observed.
- Highlight block with bright, oblique scan superimposed highlight block with bright test shows very good results.
- The chip showed a good display effect.

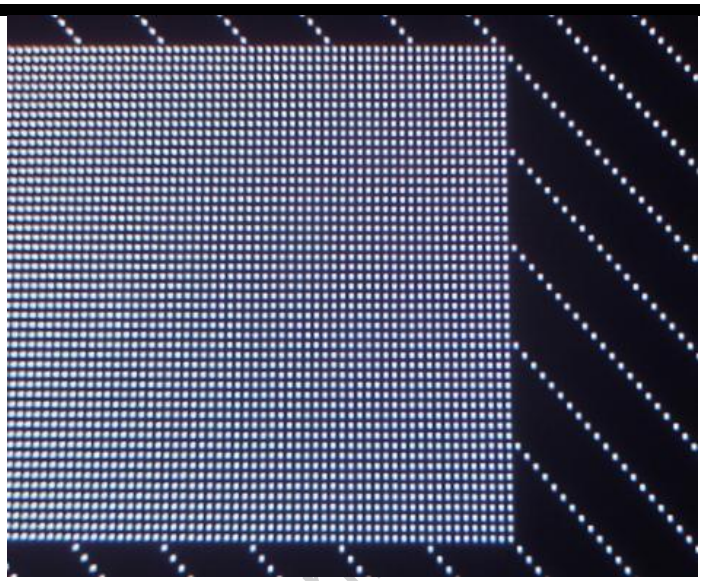


The oblique sweep ghost test showed the effect

Text ghost test shows the effect



The highlight block with the highlight test shows the effect



The oblique scan stack highlight block highlight test to show the effect

10 Directive and Register

10.1 Register Instructions

Directive name	LE	description
DATA_LATCH	1	Locch 16bit data to SRAM
DDR	2	Enter double-along mode
VSYNC	3	Update the display data
WR_CFG	5	Write register
PRE_ACT	14	Write enablement
SDR	15	Enter single-along mode

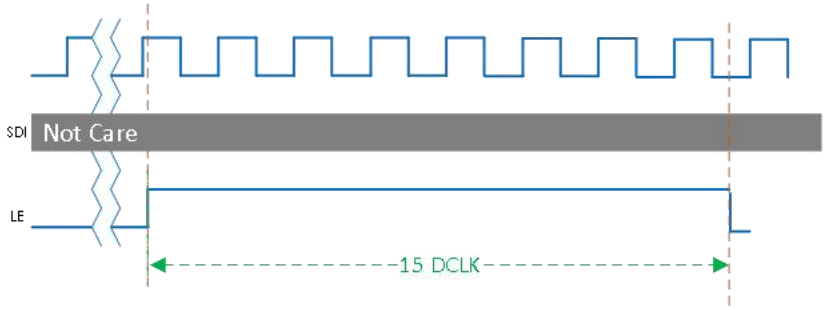
10.2 Data Command

The order of data sent	Line	channel
1	Line 0	Channel 15 (OUT15)
2		Channel 14 (OUT14)
.....		.....
16		Channel 0 (OUT0)
17	Line 1	Channel 15 (OUT15)
18		Channel 14 (OUT14)
.....		.....
32		Channel 0 (OUT0)
.....		
497	Line 31	Channel 15 (OUT15)
498		Channel 14 (OUT14)
.....		.....
512		Channel 0 (OUT0)

10.3 Single/Double Mode Switch

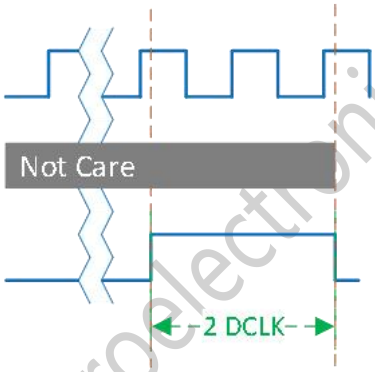
1. SDI data were sampled along the CLK ascending edge in the single mode, and SDI data were sampled along both CLK ascending edge and descending edge in the double mode.
2. The OE signal width was fixed with the CLK ascending edge count
3. The odd and double edge mode switch instruction needs to be sent once after the power-on.
4. If you need to power up into the single edge mode, you need to send the instructions shown in the

figure below



The 15 DCLK edges (rise + down) are set to SDR

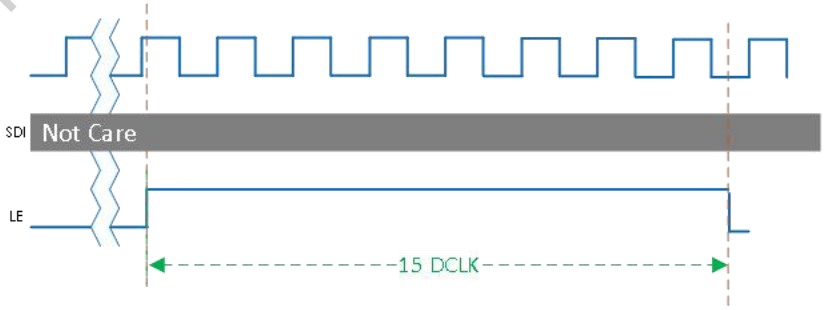
If you need to power up and enter the double edge mode, you need to send the instructions shown in the figure below



The 2 DCLK ascending edges were set to the DDR

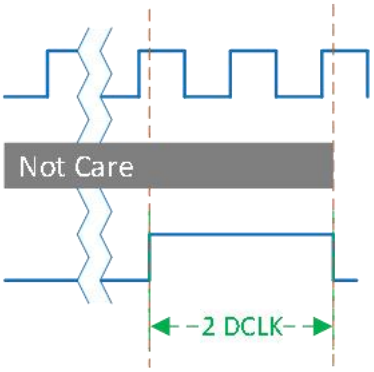
1. If the customer needs to adjust the odd and even edge during the debugging process

If you are already in the double edge mode and you need to enter the single edge mode, send the instructions in the following figure



The 15 DCLK edges (up + down) are set to SDR

If you are already in the single edge mode, you need to enter the double edge mode



2 DCLK ascending edges in single edge mode were set to DDR

10.4 Write Register

PRE _ ACT is sent first, then WR _ CFG is executed. LE is the width of 5 DCLK, the 8bit is the register address bit, and then the 8bit is the data bit of the corresponding register address.

for instance:

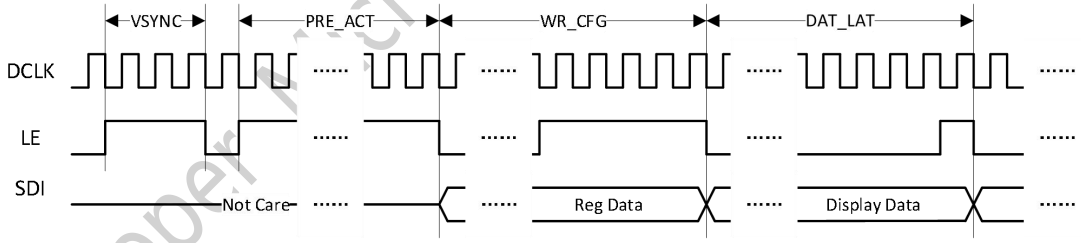
{A7, A6, A5, A4, A3, A2, A1, A0} = 8' b0000_0111;

{D7, D6, D5, D4, D3, D2, D1, D0}=8' b1001_1101;

That is, the register 0x07 (8 'b0000_0111) is set to 8' b1001_1101.

10.5 Sending Mode of the Register Signal

The specific driving mode is as follows:



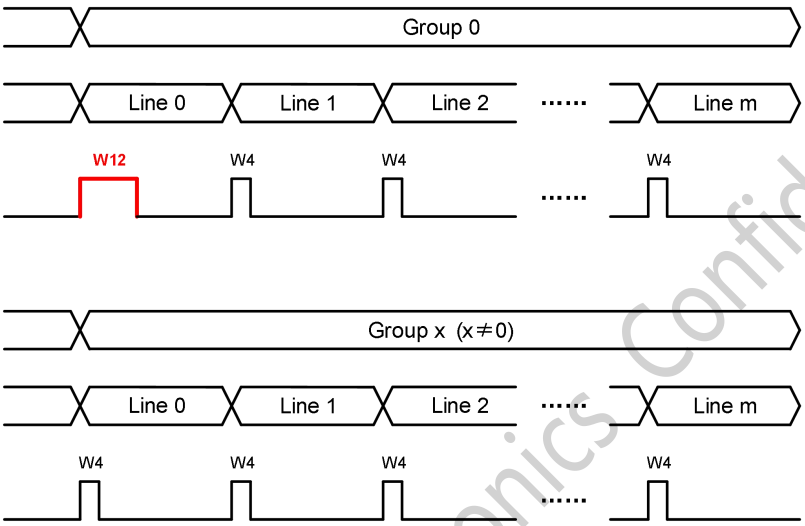
As shown in the figure above, the order of instructions and data in each frame:

1. transmit by radio VSYNC.
2. Send the PRE _ ACT.
3. Send the WR _ CFG, and write to the register configuration. Each frame can write a register value of only one address, and 15 frames can refresh all registers (a total of 15 valid register addresses) to save configuration time.
4. Send DAT _ LAT several times and write the display data with SDI.
5. The number of data sent is 16 bits.

10.6 The ROW Signal Transmission Mode

DP3254 The integrated GCLK generation circuit changes the OE signal of the universal constant current chip to ROW signal and uses ROW
The rising edge of represents the beginning of a row, where there are two types of ROW:

1. W12: The high level width representing ROW is the width of 12 DCLK
2. W4: The high level width representing ROW is the width of 4 DCLK

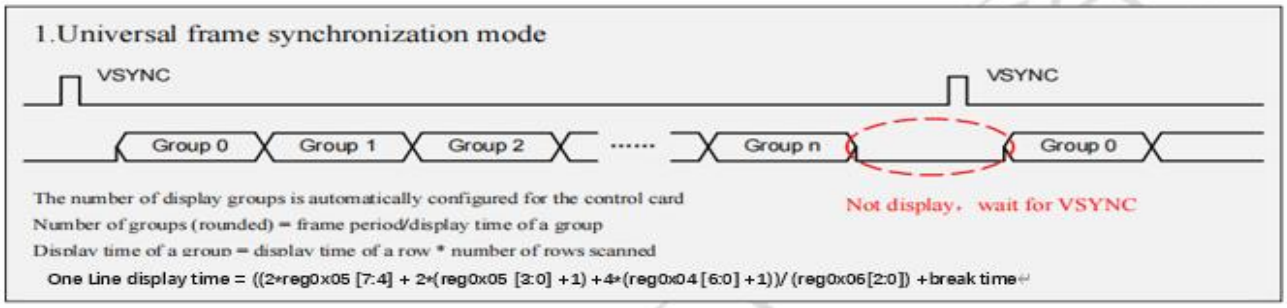


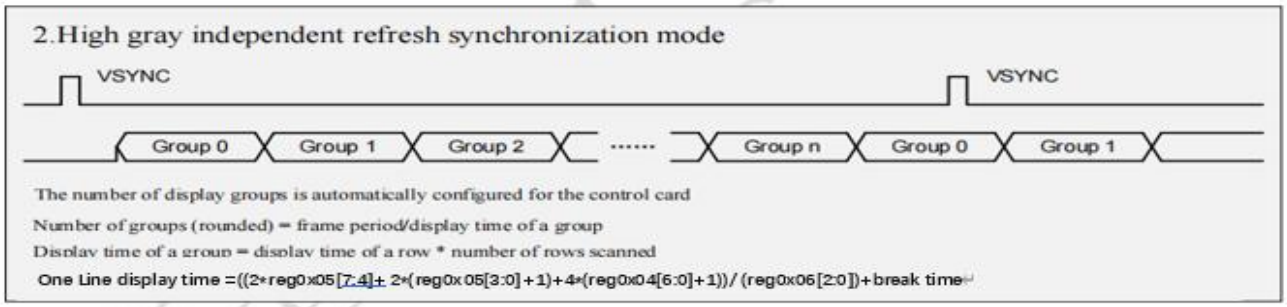
As shown in the figure above, when sending ROW signals, only the line 1 (Line 0) of group 1 (Group 0) needs to send W12 ROW signal, and other ROW signals are sent according to W4.

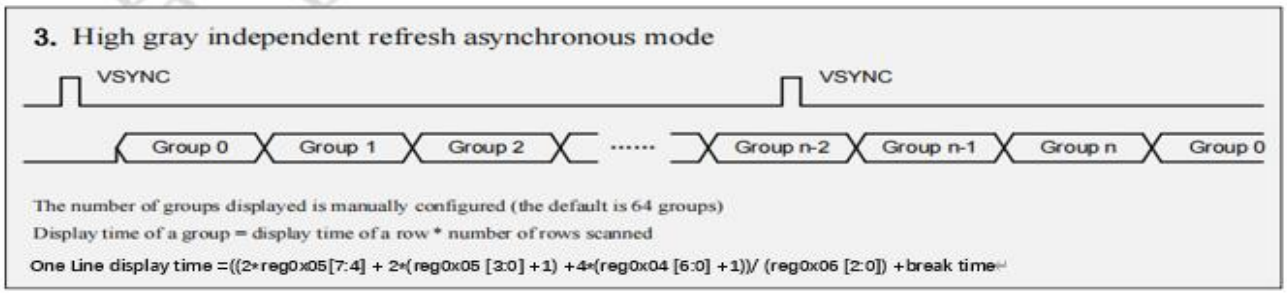
10.7 The PWM Display Mode

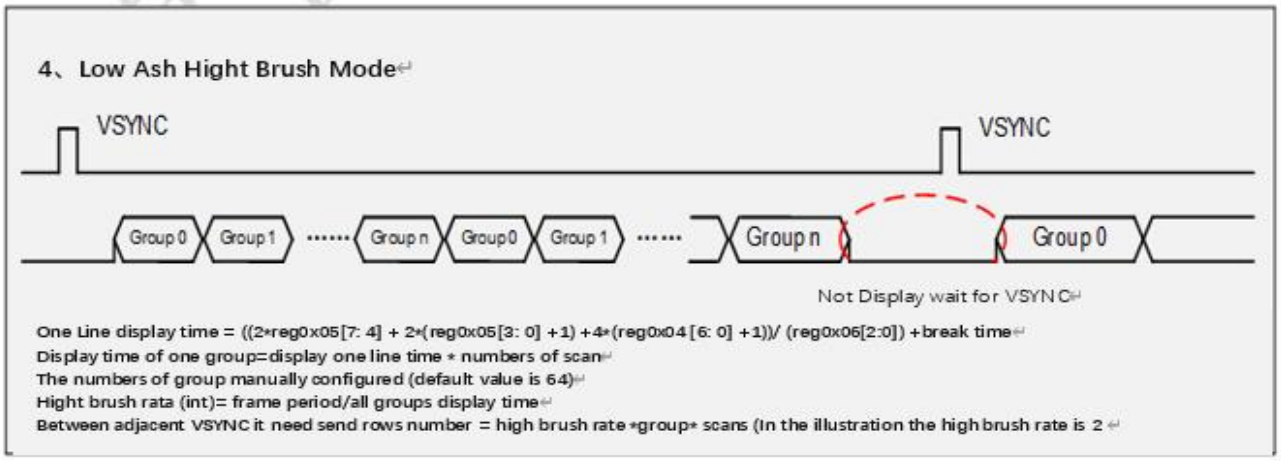
DP 3254 Four PWM display modes are integrated in the tablet:

1. General frame synchronization mode; 2. Independent refresh synchronization mode of high gray data;
3. High gray data independently refresh the asynchronous mode; 4. Low gray and high brush mode









10.7.1 General Frame Synchronization Mode

Working mode and related configuration are:

1. Configure reg0x0c [7:6] = 0 and set PWM display mode to universal frame synchronization mode
2. The number of DCLK in each line is calculated according to Eq
3. Configure the number of data groups, reg0x03 [6:0] = refresh rate / frame rate-1 (maximum of 128 sets of data supported, exceed 128 cluster register)
3. Line 1 (Line 0) of Group 1 (Group 0) is displayed after the VSYNC
4. Data display for the current frame is stopped until the arrival of the next VSYNC

10.7.2 High Gray Data Refresh Frame Synchronization Model Independently

Working mode and related configuration are:

1. Configure reg0x0c [7:6] =2, and set the PWM display mode to refresh the frame synchronization mode of the high gray data independently
2. Calculate a set of display time = frame period / (refresh rate / frame frequency)
3. Calculate the display time of a row = a set of display time / number of rows
4. The number of DCLK in each line is calculated according to the formula, which is satisfied by adjusting the series of gray scale and DCLK frequency and register reg0x6 [1:0]
5. ROW is sent continuously at a fixed display frequency. The frequency of ROW was not associated with VSYNC

Frequency of the ROW signal = 1 / row of display time = 1 / time between two ROW rise edges

6. Group 0, line 0, sends the ROW signal of W12, and sends the W4 ROW signal in other cases

Each ROW signal (group * row scans) has only one W12 and cycles in this manner.

10.7.3 High-gray data Independently Refreshes Asynchronous Mode

Working mode and related configuration are:

1. Configure reg0x0c [7:6] =3, and set the PWM display mode to refresh the asynchronous mode of the high gray data independently
2. The number of DCLK in each line is calculated according to Eq

The number of displayed data groups was manually configured, by default to 64 groups (reg0x03 [6:0] =7'h3f).

3. ROW is sent continuously according to fixed display frequency. The frequency of ROW was not associated with VSYNC

Frequency of the ROW signal = 1 / row of display time = 1 / time between two ROW rise edges

4. Group 0 row 0 sends ROW signal W12, and otherwise sends ROW signal W4 signal

Each ROW signal (group (per register configuration) * row scan) has only one W12 and cycles in this manner. The number of times you can cycle in a frame is unlimited

5. Visual refresh rate =1 / (display time * sweeps of a row)

10.7.4 Low-grey and High-brush Mode

Working mode and related configuration are:

1. Configure reg0x0c [7:6] = 1 and set PWM display mode to low gray high brush mode

2. The number of display groups is manually configured (the default configuration is 64 groups)
3. The number of DCLK in each line is calculated according to the formula, and the display time of one row is calculated
4. Calculate a set of display time = one row display time * number of rows
5. Calculate all groups display time = one group display time * number of groups,
6. High brush rate (consolidation) = frame period / display time of all groups
7. Two Vsync before you need to send a high brush rate * display number of groups * scan several ROW signals
8. Line 1 (Line 0) of Group 1 (Group 0) is displayed after the VSYNC
9. The data of the current frame shows high brush times and stops the display until the next VSYNC arrives
10. Visual refresh rate = frame rate * number of data groups * high brush rate = (3840 / 7680Hz) * high brush rate
11. The low gray and high brush mode only needs to change the ROW signal according to the above steps, and the gray level does not need to be adjusted

10.8 Relevant Configuration of PWM Display

10.8.1 Row Scan Number Configuration

DP3254 Maximum support of 32 row sweeps, configured as reg0x02 [5:0] = number of row scans-1

10.8.2 Line gray-scale Series Configuration

reg0x04 [6:0] represents the PWM display length of a row, the PWM display length of a row = 4 * (reg0x04 [6:0] + 1) with maximum support of 64X4=256

For example, if the configuration line gray scale level is 128, then set reg0x04 [6:0] =7'h1f=31

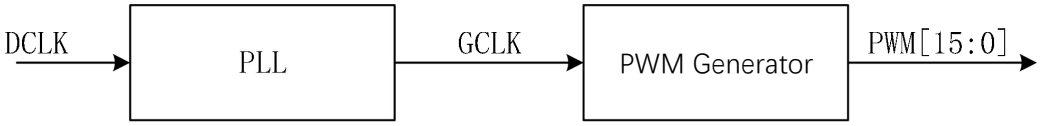
10.8.3 PWM Display Packet Configuration

reg0x03 [6:0] shows groups for PWM, and PWM = reg0x03 [6:0] + 1, and the maximum number of supported groups is 128 groups

In frame synchronization mode, PWM displays packet number = refresh rate / frame rate, configuration reg0x03 [6:0] = refresh rate / frame rate-1

In asynchronous mode, PWM display groups can be configured independently (regardless of refresh rate)

10.8.4 Internal Grayscale Clock Configuration



DP3254 Integrated PLL produces the gray scale clock GCLK, and the relevant calculation formula is as follows:

FGCLK=FDCLK*(reg0x06[2:0]+1)

10.8.5 PWM Gray Series & Gamma Generation

PWM gray scale (maximum) * PWM display group =4 * (reg0x04 [6:0] + 1) * (reg0x03 [6:0] + 1) -1

for example:

reg0x04[6:0]=7’ h7f, reg0x03[6:0]= 7’ h7f

PWM gray series (maximum) =4 * (127 + 1) * (127 + 1) -1=65535=16bit

Gamma can be calculated and generated according to the PWM gray scale series (maximum value) (this part is generated by the control card manufacturer according to its own gamma generation formula)

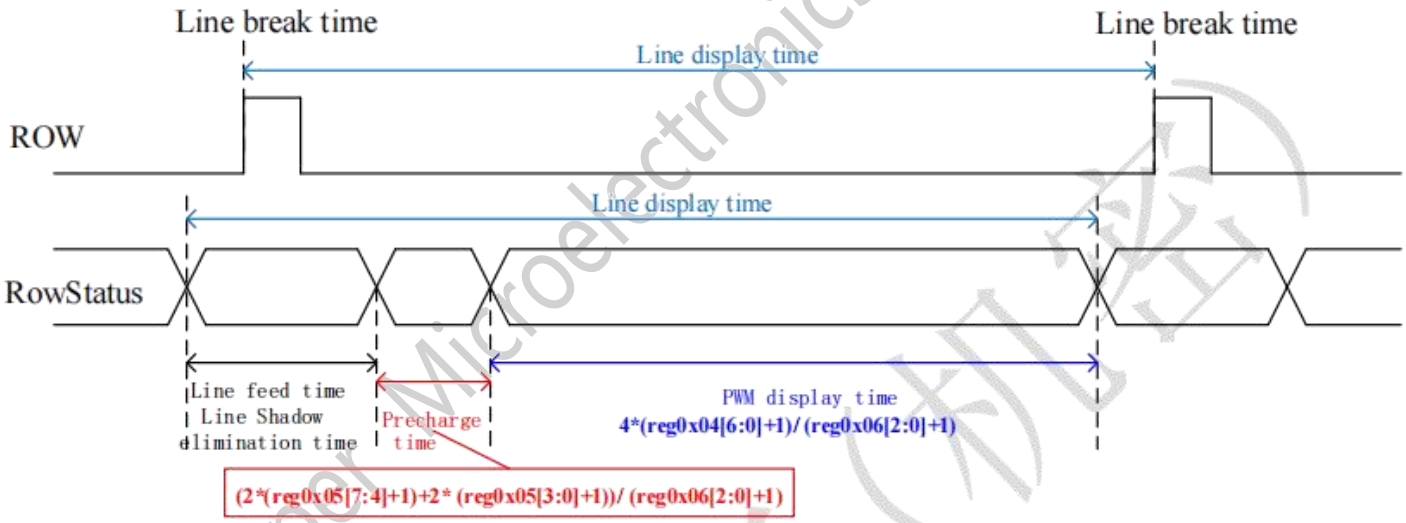
Up to 16bit only (low 16-bit valid)

10.8.6 Calculated the Display Time for Each Row

The display time of each row is represented by the number of DCLK, using the calculation formula:

(2 * (reg0x05 [7:4] + 1) + 2 * (reg0x05 [3:0] + 1) + 1 * + 4 * (reg0x04 [6:0] + 1)) / (reg0x06 [2:0] + 1) + Line change time

Note: The results of the above formula are rounded up



10.9 Open Circuit Detection and Removal of Bad Spots

Check [remove bad points]: reg0x0c[1] =1;

Do not check [remove bad points]: reg0x0c[1] =0

Open-circuit detection timing:

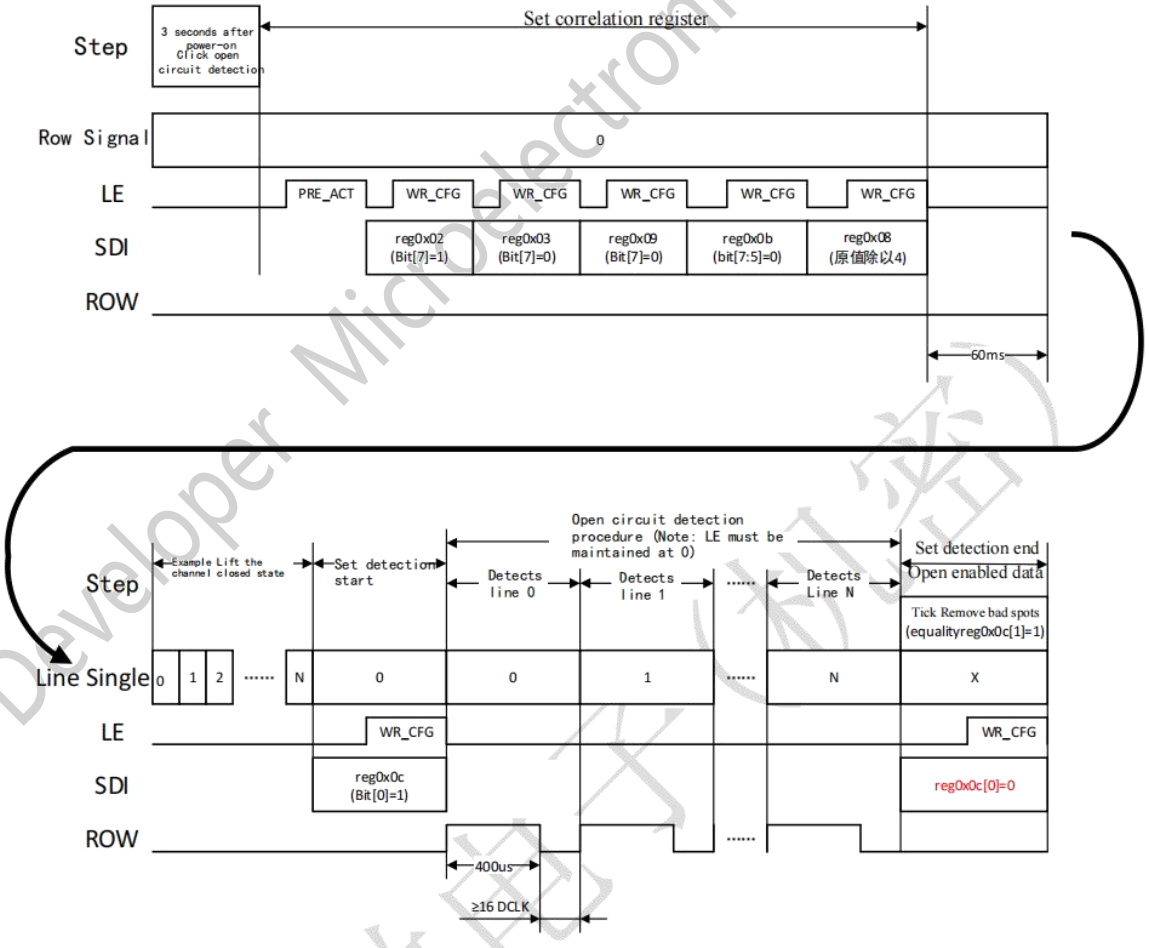
1. Perform open circuit detection after 3 seconds or click open circuit detection.
2. Configure reg0x02[7] =1, reg0x03[7] =0 (enable open circuit detection mode)

   Configuration reg0x0b [7:5] =0 (Configure constant current inflection point to the lowest)

   Configure reg0x08 [7:0] right move two bits, high fill 0 (configured output current is 25% of normal

current)

3. Change to line 0 and stop all row signals for one frame (60ms)
4. Change the line signal, quickly scan from line 0 to the last line, and then return to line 0 (this step is mainly to avoid the output channel of the driver chip).
5. Configure reg0x0c[0] =1 (open open circuit detection mode)
6. Send Row signal, that is, set ow to high, then ROW to low, high level time (400us recommended) as the time required to detect a row, and low level time (16 DCLK recommended) as the data acquisition and latching time.
7. Change lines by scanning as many lines as step 6 does. The change time recommended alignment with the rising edge of the ROW.
8. After detection, configure reg0x0c[0] =0 (close open circuit detection mode), reg0x0c[1] =1 (when checked [remove bad point]).
9. During open circuit detection, LE=0, DCLK is normally sent continuously (at least 128 DCLKs are guaranteed between two ROWs).



10.10 Register

register	Register function name	Register function description and default values
0x02		R：2A G：2A B：2A
7	OPDET_EN_A1	OPDET _ EN _ A 1 is highly efficient; it must cooperate with OPDET _ EN _ A 2, OPDET _ EN _ A 3
6		Reserved
5:0	LINE_SET<5:0>	Scan lines = LINE _ SET + 1
0x03		R：3F G：3F B：3F
7	OPDET_EN_A2	OPDET _ EN _ A 2 is low effective; cooperate with OPDET _ EN _ A 1, OPDET _ EN _ A 3
6:0	GROUP_SET<6:0>	Show the refresh rate = REG 03 <6:0> + 1
0x04		R：20 G：20 B：20
7		Reserved
6:0	PWM_WIDTH<6:0>	Number of row GCLK
0x05		R：34 G：34 B：34
7:3	DISSHD_TIME_1<3:0>	Shadow time-level 0 ~15 levels, a total of 16 levels, the default value is 0
2:0	DISSHD_TIME_2<3:0>	Muuation time-0 ~15, a total of 16
0x06		R：42 G：42 B：42
7:3	DECOUP_RAT<4:0>	Coupling optimization coefficient
2:0	PLL_DIV<2:0>	GCLK frequency doubling 0:1 Times frequency 1:2 Times frequency 2:3 Times frequency 3:4 Times frequency
0x07		R：00 G：00 B：00
7	Gamma_COARSE_EN	Gamma coarse tuning switch-1: on 0: off
6:4	Gamma_COARSE<2:0>	Gamma-0-7, a total of 8
3	Gamma_FINE_EN	Gamma fine switch-1: fine on 0: fine off
2:0	Gamma_FINE<2:0>	Gamma fine tuning level-0~7 level, a total of 8 levels
0x08		R：7F G：7F B：7F
7:0	IGAIN<7:0>	The reg 08 [7:6] is the 50% progressive bit of the current gain reg08[5:0]= round (128*IGAIN/(reg08[7:6]+1))-1
0x09		R：60 G：60 B：60
7	EN_IR	0: Resistance; 1: no resistance
6:5		Reserved
4:0	DECOUP_1<4:0>	Coupled optimization level 1-0 to 31, a total of 32 levels
0x0a		R：BE G：BE B：BE
7:6	DECOUP_ENHANCE<1:0>	Coupled optimization enhancement rank – successively weakened from 0 to 3
5		Reserved
4	DISSHD_EN	Muuation rating switch-on: 1 off: 0

3	DECOUP_EN	Coupling optimization switch
2:1	PIT_OPT<1:0>	Low gray point optimization-0 ~3, a total of 4 levels, default level 3
0	LG_ENHANCE	Low gray display effect enhancement switch
0x0b		R：28 G：30 B：31
7:5	CORNER <2:0>	Constant current output inflection point level 0: Low turn (0.18 V-0.3 V) corresponds to the current range of 0.5 mA ~ 18 mA 1: The corresponding current range of non-low turn (0.3 V-0.45 V) is 0.5 mA ~ 25 mA
4:0	DISSHD_LEVEL<4:0>	Shadow level, level 0 ~31 level, a total of 32 levels
0x0c		R：90 G：90 B：90
7:6	SYNC_MODE<1:0>	0: Frame synchronization mode 1: Low gray and high brush mode 2: High gray data independently refresh the synchronization mode 3: High gray data independently refresh the asynchronous mode
5:4	LP_MODE<1:0>	Energy saving mode 0: Dynamic energy saving 1: Dynamic energy saving + black screen energy saving mode 1-Performance priority 2: Dynamic energy saving + black screen energy saving mode 2-Low power consumption first 3: Dynamic energy saving + black screen energy saving mode 3-Very low power consumption
3:2		Reserved
1	RM_OP	Remove the bad point function switch
0	OPDET_EN	When the conditions OPDET _ EN _ A 1 and OPDET _ EN _ A 2 are met simultaneously, open OPDET _ EN to enter the open circuit detection mode
0x0d		R：08 G：12 B：18
7:5		Reserved
4:0	DECOUP_LEVEL<4:0>	Coupled optimization level, level 0 to 31, a total of 32 levels
0x0e		R：00 G：00 B：00
7:6		Reserved
5	PRECHA_EN	Enable the coupling optimization of 2
4:0	VS_PRECHA	Coupled optimization level 2-0 to 31, a total of 32 levels
0x0f		R：00 G：00 B：00
7		Reserved
6:0	IGAINL	'No resistance current adjustment range + / -7.5%, step length 0.5%
0x10		R：00 G：00 B：00
7:0		Reserved
0x11		R：00 G：00 B：00

7	OPEN_EN_B	Enable the coupling optimization of 1
6:0		Reserved
0x12		R：00 G：00 B：00
7:0		Reserved
0x13		R：00 G：00 B：00
7:0		Reserved
0x14		R：00 G：00 B：00
7:0		Reserved
0x15		R：00 G：00 B：00
7:0		Reserved
0x16		R：00 G：00 B：00
7:0		Reserved
0x17		R：00 G：00 B：00
7:0		Reserved

11 Encapsulation Cooling power (P_D)

The maximum heat dissipation power of the package body is determined by the formula $P_{D(\max)} = \frac{(T_j - T_a)}{R_{th(j-a)}}$

When all the 16 channels are opened, the actual power is:

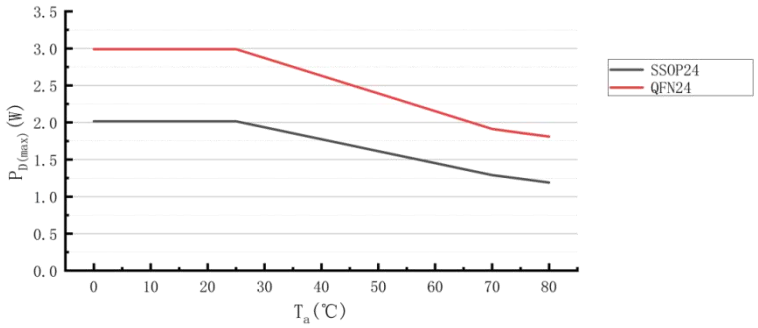
$$P_{D(act)} = I_{DD} * V_{DD} + I_{OUT} * Duty * V_{DS} * 16$$

To ensure that $P_{D(act)} \le P_{D(max)}$ The relationship between the maximum current and duty ratio is:

$$I_{OUT(max)} = \frac{\frac{T_j - T_a}{R_{th(j-a)}} - (I_{DD} * V_{DD})}{V_{DS} * Duty * 16}$$

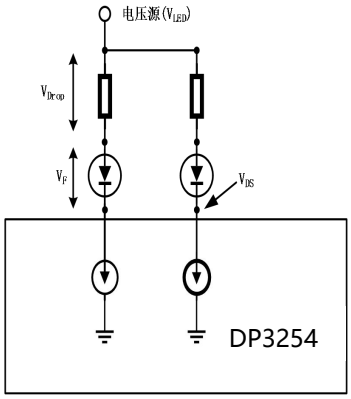
among T_j For the junction temperature (T_j=150℃）， T_a For the ambient temperature, and V_{DS} Is the constant current output port voltage, Duty is the duty cycle, $R_{th(j-a)}$ For the package of the thermal resistance.

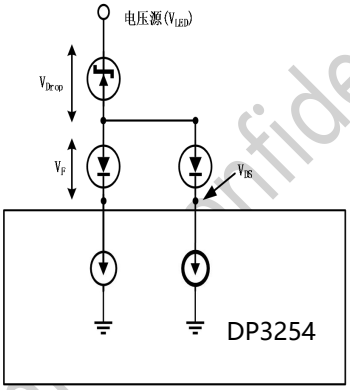
package	$R_{th(j-a)}$(℃/W)	$P_{D(max)}$(W)
QSOP24	62	2.01
QFN24	41.8	2.99



12 Load Terminal Voltage (VLED)

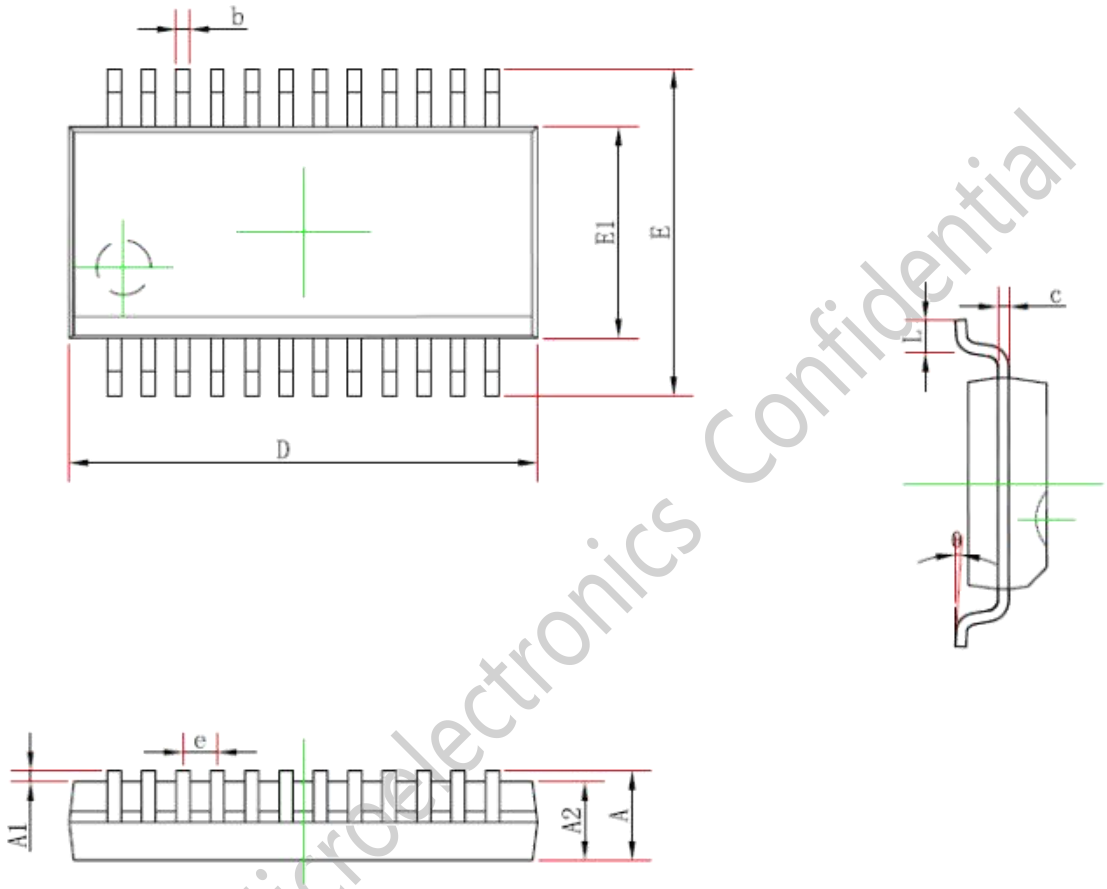
In order to optimize the heat dissipation capacity of the package, the output voltage (V_{DS}) The best operating range is 0.3V~1.0V (now I_{OUT}=0.5 ~ 36mA)。if $V_{DS}=V_{LED}-V_F$a word used in a person's name V_{LED}=5V, when too high output voltage (V_{DS}) May result cause $P_{D(act)} > P_{D(max)}$; In this case, it is recommended to use a low V as low as possible$_{LED}$Voltage for use, can also be used as an external string resistance or voltage regulator tube as V_{DROP}. At the moment lead to $V_{DS}=(V_{LED}-V_F)-V_{DROP}$, To reduce the input voltage (V_{DS}) The effect of the value. The application diagram of the external string resistance or voltage regulator pipe can be referred to in the following figure.





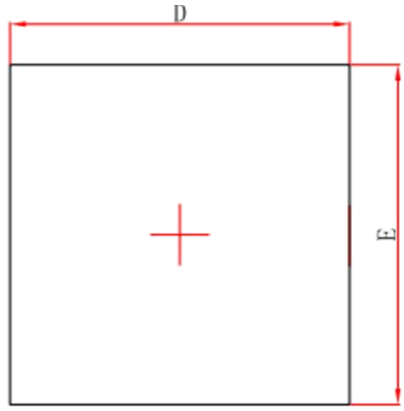
13 Encapsulation information

- QSOP24 Plastic sealing specification drawing

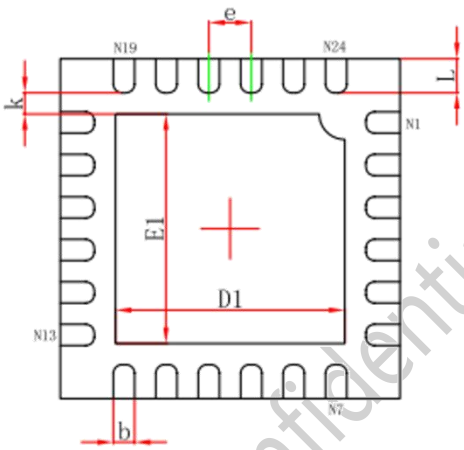


	millimetre (mm)	
	least value (Min)	crest value (Max)
A	—	1.95
A1	0.05	0.35
A2	1.05	—
b	0.1	0.4
c	0.05	0.254
D	8.2	9.2
E1	3.6	4.2
E	5.6	6.5
e	0.635TYP	
L	0.3	1.5
θ	0°	10°

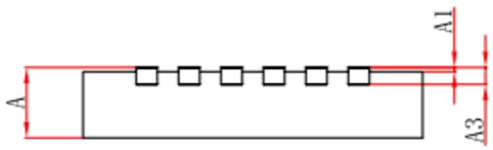
- QFN 24 plastic seal specification drawing



Top View



Bottom View



Side View

	millimetre (mm)	
	least value (Min)	crest value (Max)
A	0.700/0.800	0.800/0.900
A1	0.000	0.050
A3	0.203REF	
D	3.924	4.076
E	3.924	4.076
D1	2.6	2.8
E1	2.6	2.8
k	0.20MIN	
b	0.200	0.300
e	0.500TYP	
L	0.324	0.476

14 Official Announcement

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