# DP3252 16 Channel 16 scans Low-turning PWM Constant Current Driver

## 1 OVERVIEW

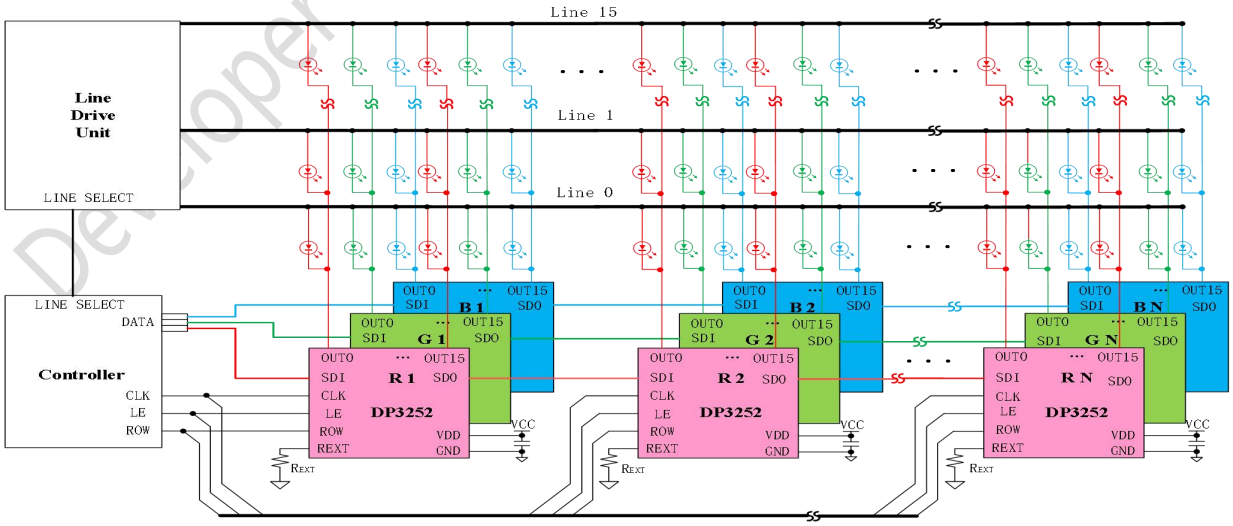
DP3252 is a 16-channel low-transition PWM constant-current drive chip designed for LED displays. It integrates high-precision current generation circuit technology on-chip, so that the current error between chips can be controlled within 2.0%, and the new low-gray and high-brush mode is added to improve low-gray refresh rate. And integrated with a number of lifting LED display, the exclusive technology of display effect can bring more improvements.

## 2 FEATURES

- Power supply voltage range：2.6～5.5V
- Operating temperature range：-40℃～85℃
- Scanned area：1 ~ 16 scans，arbitrarily adjustable
- 16 constant current output channels
- Support non-external resistor mode
- Constant current output range
  - 0.5mA～18mA （$V_{out}$=0.3V）
  - 0.5mA～40mA （$V_{out}$=0.45V）
- Inter-channel current error
  - Typical value：± 1.2% Max：± 2.5% ($V_{out}$=0.45V)
- Inter-chip current error
  - Typical value：±1.5% Max：±2.0%
- High gray independent refresh, no interframe black field
- Low gray high brush, low gray supports 1~8 times display frame rate
- The highest refresh rate supports 128 times frame rate (7680Hz)
- Optimize the display state
  - improve low gray uniformity improve the first line darkening
  - improve up and down ghosting
  - improve high-low gray coupling
  - improve cross-panel coupling
- Integrated PLL produces internal GCLK with lower EMI
- Encapsulation mode：QSOP24/QFN24
- Excellent ESD features

## 3 APPLICATION FIELDS

- High refresh rate LED video display
- Monochrome two-color or full- color LED display
- High density and small pitch LED panel display




DP3252 Typical Application Schematic

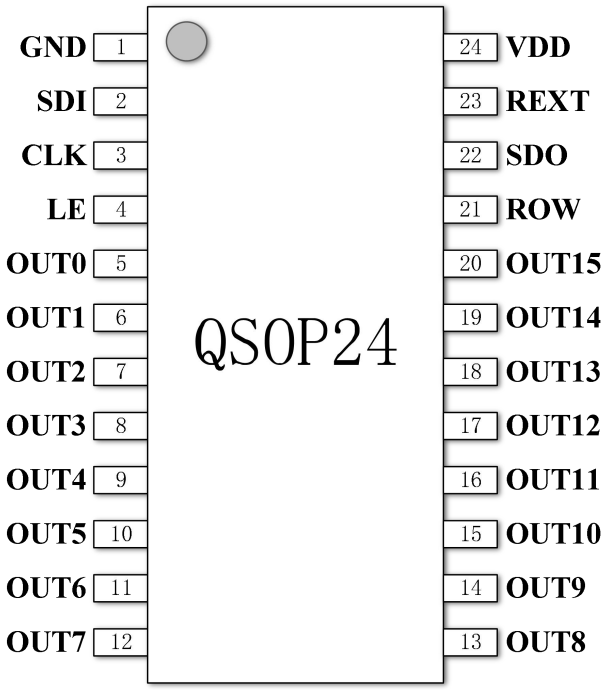
# CONTENT

# REVISION RECORD

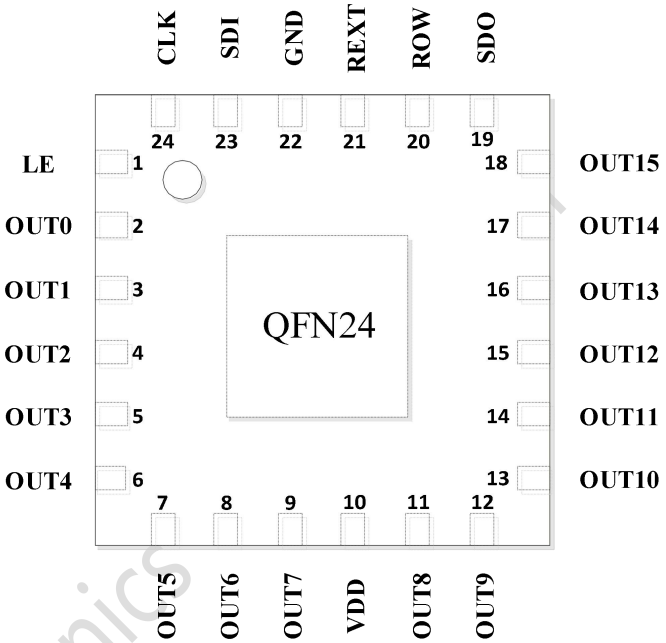
| Version | Date | Reviser | Revised Contents |
|---|---|---|---|
| V0.1 | 2023.07 | Wangmei | Original Version |
| V0.2 | 2023.08 | Wangmei | Modify instructions and registers |

# 4 PRODUCTS DESCRIPTION

- Pin Definition




QSOP24 Pin Definition Diagram




QFN24 Pin Definition Diagram

- Pin Description

| QSOP24 Pin No. | QFN24 Pin NO. | Pin Name | Pin Description |
|---|---|---|---|
| 1 | 22 | GND | Chip Grounding Terminal |
| 2 | 23 | SDI | Serial Data Input Terminal |
| 3 | 24 | CLK | Serial Clock Input |
| 4 | 1 | LE | Data and Instruction Latch End, different LE length represents different instructions |
| 5 ~ 20 | 2 ~ 9 11 ~ 18 | OUT0 ~ OUT15 | Constant Current Output Terminal |
| 21 | 20 | ROW | Row Switching Signal |
| 22 | 19 | SDO | Serial Data Output |
| 23 | 21 | REXT | Connect the External Resistance Terminal |
| 24 | 10 | VDD | Chip Power Terminal |

- Product Purchase Information

| Product Name | Encapsulation mode | Packing Method | Quantity/Disc | Humidity Level |
|---|---|---|---|---|
| DP3252 | QSOP24 | Tape | 4000 | MSL=3 |
| | QFN24 | Tape | 5000 | |

- Product Marking


QSOP24

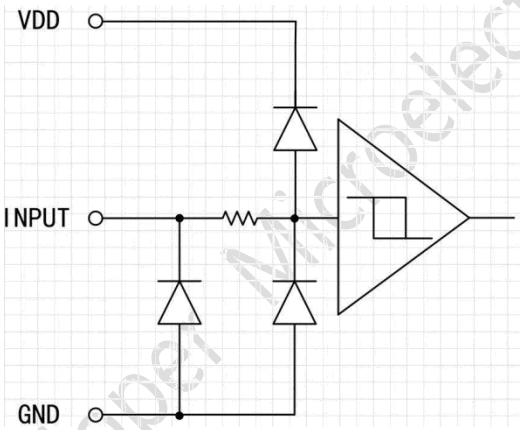

QFN24

DP3252 is the product name
XXXXXX represents th product batch number

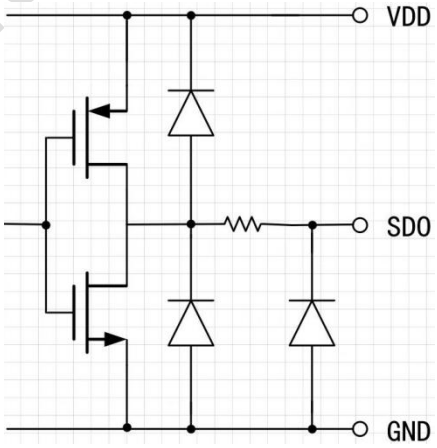
# 5 SCHEMATIC CIRCUIT DIAGRAM

## 5.1 INPUT/OUTPUT EQUIVALENT CIRCUIT

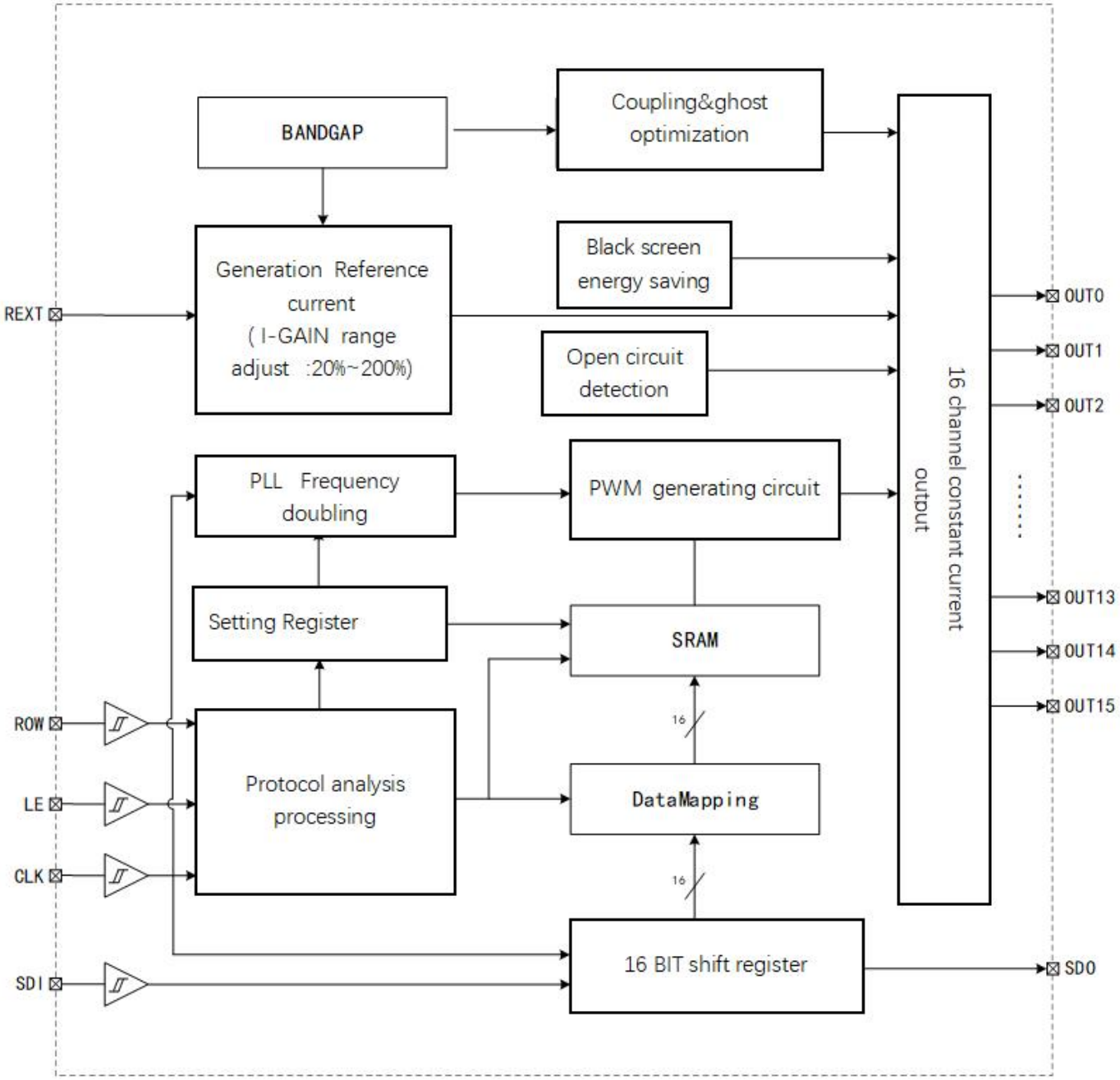
SDI, CLK,LE,OE Input terminal




SDO Output terminal



## 5.2 INTERNAL CIRCUIT BLOCK DIAGRAM




A Schematic diagram of the internal circuit

# 6 PARAMETER LIST

## 6.1 MAXIMUM LIMIT PARAMETER

| Project | Symbol | Rated Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 0 ~ 5.5 | V |
| Output Current | $I_O$ | 40 | mA |
| Input Voltage | $V_{IN}$ | -0.4 ~ $V_{DD}$+0.4 | V |
| Output withstand voltage | $V_{OUT}$ | 11 | V |
| clock frequency | $F_{CLK}$ | 25 | MHz |
| Operating Temperature | $T_{opr}$ | - | - |
| Storage Temperature | $T_{stg}$ | -55 ~ 150 | ℃ |

- All voltage values are based on the chip grounding terminal (GND) as a reference point, and the test temperature for the maximum limit parameter is 25℃.
- If the actual working conditions exceed the specified value may cause permanent damage to the components; If the actual operating conditions are slightly below the maximum and work for a long time, the reliability of the component may be reduced. The above values are only partially specified, and this product does not support functional operation under other conditions outside the specifications.
- The maximum peak welding temperature of surface paste products shall not exceed 260℃. The temperature curve shall be set by the factory according to J-STD-020 standard, the actual situation of the factory and the solder paste manufacturer's suggestion.

## 6.2 ESD RATING

### 6.2.1 CONTACT ESD

| Symbol | Condition | | Min Value | Typical Value | Max Value | Unit |
|---|---|---|---|---|---|---|
| $V_{(ESD)}$ | Human-body model (HBM) [1] | OUTn Pin-GND | - | - | - | kV |
| | | OTHER Pin-GND | - | - | - | kV |
| | Machine Mode (MM) [2] | OUTn Pin-GND | - | - | - | kV |
| | | OTHER Pin-GND | - | - | - | kV |

- [1]The minimum HBM model ESD voltage for all pins complies with the Class-3B standard of JEDEC JS-001-2017 document.
- [2] The minimum MM model ESD voltage for all pins complies with the Class-C standard in JEDEC EIA/JESD22-A115C document.

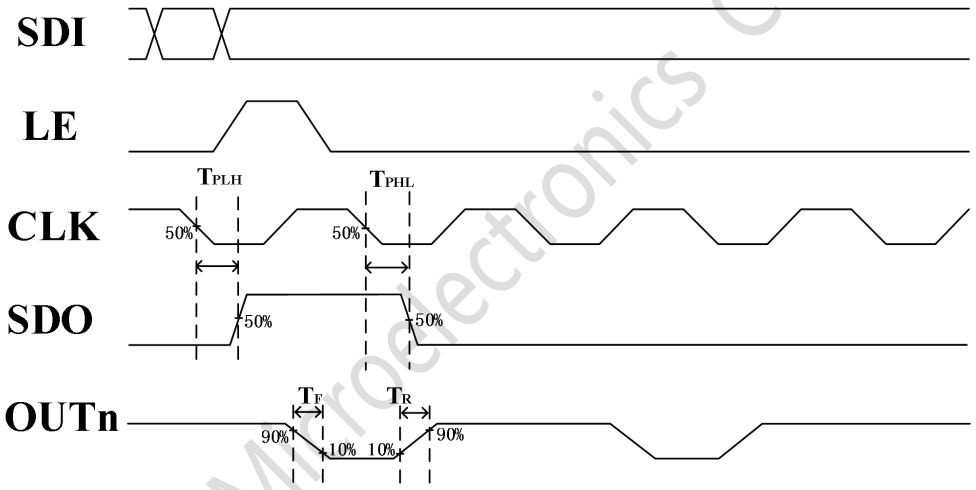
## 6.3 ELECTRICAL CHARACTERISTICS (Unless otherwise specified,VDD=3.5V~5V，Ta=25℃)

| Project | | Symbol | Test Circuit | Test Condition | | Mini Value | Typical Value | Max Value | Unit |
|---|---|---|---|---|---|---|---|---|---|
| REXT voltage characteristics | | VR_TT | 1 | $V_{DD}$=5V,$R_{EXT}$=1K IGAIN=100%,$T_a$=25℃ | | - | 1.533 | - | V |
| | | VR_LT | | $V_{DD}$=5V $R_{EXT}$=1K IGAIN=100% | $T_a$=-40℃ | - | 1.56 | - | V |
| | | VR_HT | | | $T_a$=85℃ | - | 1.495 | - | V |
| | | VR_LV | | $T_a$=25℃ $R_{EXT}$=1K IGAIN=100% | $V_{DD}$=5.5V | - | 1.535 | - | V |
| | | VR_HV | | | $V_{DD}$=2.6V | - | 1.521 | - | V |
| Constant current output inflection point | | $V_{OUT1}$ | 2 | $V_{DD}$=5.0V $R_{EXT}$=1k 拐点等级 0 | IOUT=18mA | - | 350 | - | mV |
| | | $V_{OUT2}$ | | | IOUT=9mA | - | 290 | - | mV |
| | | $V_{OUT3}$ | | | IOUT=4.5mA | - | 260 | - | mV |
| | | $V_{OUT4}$ | | $V_{DD}$=5.0V $R_{EXT}$=1k 拐点等级 1 | IOUT=18mA | - | 460 | - | mV |
| | | $V_{OUT5}$ | | | IOUT=9mA | - | 390 | - | mV |
| | | $V_{OUT6}$ | | | IOUT=4.5mA | - | 360 | - | mV |
| Constant current source output range | | IOUT | 2 | 拐点等级 0 | | 0.5 | - | 18 | mA |
| | | IOUT1 | | 拐点等级 1 | | 0.5 | - | 40 | mA |
| Inter-chip output current error | | DCHIP | 2 | VDS=0.6V | | — | ±1.5 | ± 2.0 | % |
| Output current error between channels | | DCHL | 2 | VDS=0.6V | | — | ± 1.2 | ±2.5 | % |
| Constant current error/VDS variation | | %/ΔVDS | 2 | VDS=0.3~3.0V | | — | — | ± 1.0 | %/V |
| Constant current error /VDD variation | | %/ΔVDD | 2 | VDD=3.5V~5.0V | | — | — | ± 1.0 | %/V |
| output voltage at ON | | $V_{O(ON)}$ | 2 | OUT0~OUT15 | | 0.3 | - | $V_{DD}$ | V |
| SDO drive current | High Level | IOH | 3 | VDD=5V | | — | -22 | — | mA |
| | Low Level | IOL | | | | — | 23 | — | mA |
| Output Level | High Level | VOH | 4 | IOH=-1mA | | 4.6 | — | — | V |
| | Low Level | VOL | | IOL=1mA | | — | — | 0.4 | V |
| High level logistic | | $V_{IH}$ | 5 | - | | 0.7*$V_{DD}$ | - | $V_{DD}$ | V |

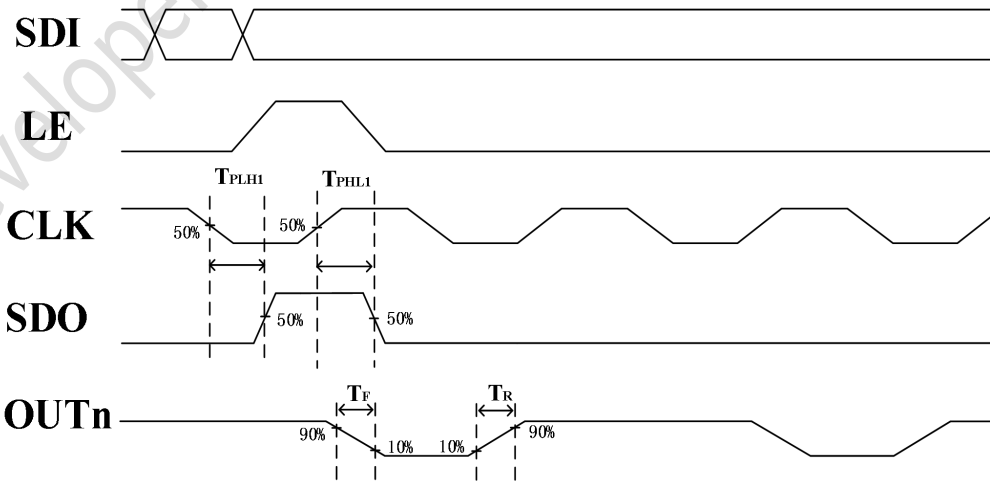
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| input voltage | | | | | | | |
| Low level logistic input voltage | $V_{IL}$ | | - | GND | - | $0.3*V_{DD}$ | V |
| Supply current (with resistance) (White screen power consumption) | $I_{DD1}$ | 6 | $R_{EXT}$=3K，White Screen IOUT=6mA，Refresh rate 3840 | - | 4.69 | - | mA |
| Supply current (with resistance) (Black screen energy-saving power consumption) | $I_{DD3}$ | 6 | $R_{EXT}$=3K，Black Screen IOUT=6mA，Capability Priority | - | 2.95 | - | mA |
| | $I_{DD4}$ | | $R_{EXT}$=3K，Black Screen IOUT=6mA，Low power consumption priority | - | 1.29 | - | mA |
| | $I_{DD5}$ | | $R_{EXT}$=3K，Black Screen IOUT=6mA，lowest power consumption | - | 0.68 | - | mA |
| Power supply current (no resistance) (White screen power consumption) | $I_{DD1}$ | 6 | White Screen IOUT=6mA，Refresh Rate 3840 | - | 4.26 | - | mA |
| Power supply current (no resistance) (Black screen energy-saving power consumption) | $I_{DD3}$ | | Black Screen IOUT=6mA，Capability Priority | - | 2.88 | - | mA |
| | $I_{DD4}$ | | Black Screen IOUT=6mA，Low power consumption priority | - | 1.45 | - | mA |
| | $I_{DD5}$ | | Black Screen IOUT=6mA，lowest power consumption | - | 0.79 | - | mA |

## 6.4 DYNAMIC CHARACTERISTICS (Unless otherwise specified，VDD=3.5V～5V，Ta=25℃)

| Project | Symbol | Test Circuit | Test Condition | Mini Value | Typical Value | Max Valule | Unit |
|---|---|---|---|---|---|---|---|
| CLK-SDO delay | TPHL | 7 | VDD=5V, FDCLK=12.5MHz | - | 15 | - | ns |
| CLK-SDO delay | TPLH | | | - | 15 | - | ns |
| CLK-SDO delay | TPHL1 | | | - | 25 | - | ns |
| CLK-SDO delay | TPLH1 | | | - | 15 | - | ns |
| Constant Current Output Rise Time | TR | | IOUT=10mA, ΔVOUT=3V | - | 65 | - | ns |
| Constant current output drop time | TF | | | - | 50 | - | ns |




Single along time series waveform diagram

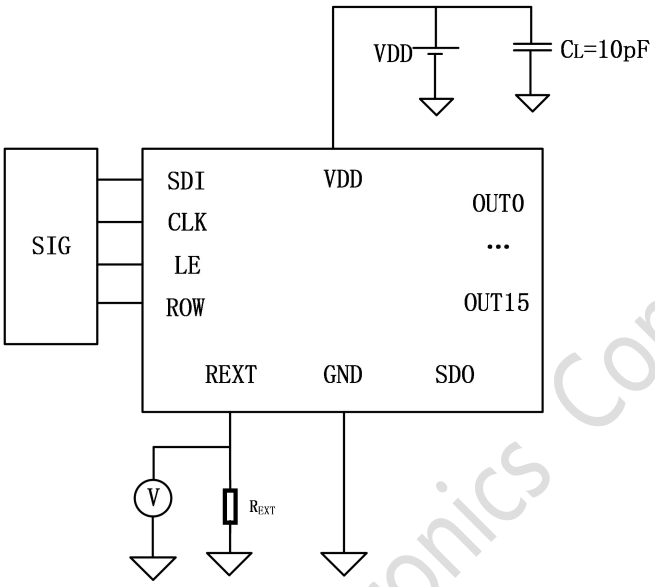



Double along time sequence waveform diagram

# 7 TEST CIRCUIT DIAGRAM

## 7.1 TEST CIRCUIT 1

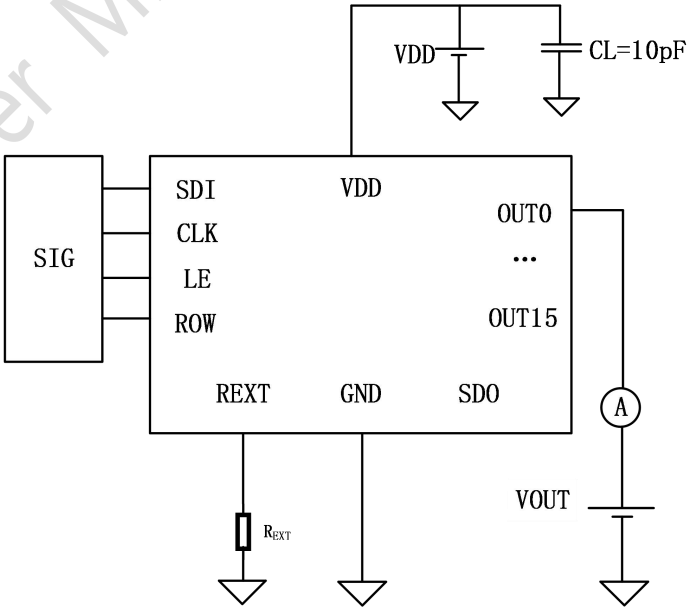
- External resistance voltage




Test circuit 2 schematic diagram

## 7.2 TEST CIRCUIT 2

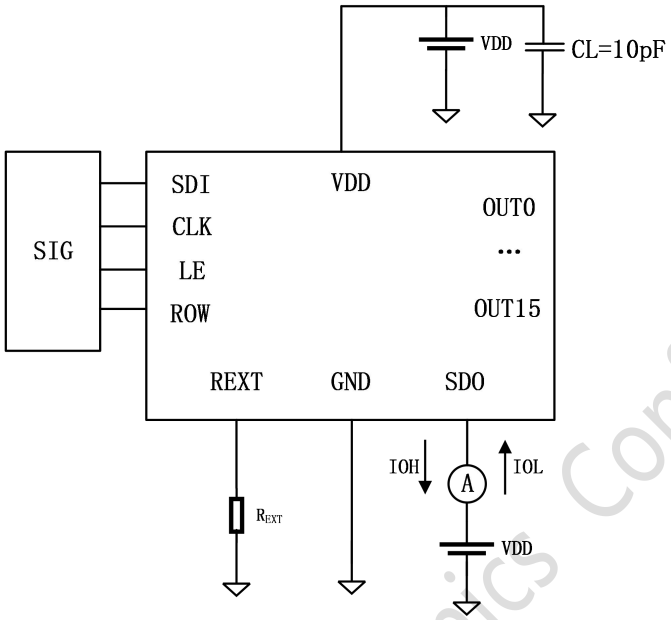
- Constant current output inflection point voltage & corresponding inflection point current (under open circuit detection)




Test circuit 2 schematic diagram

## 7.3 TEST CIRCUIT 3

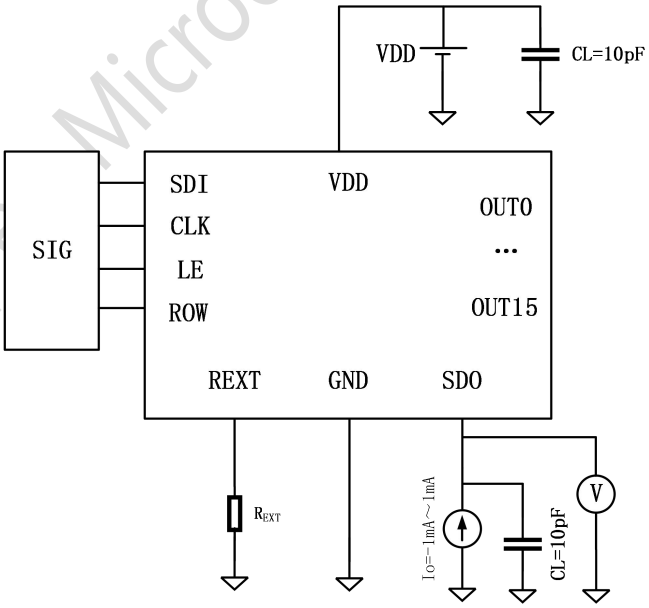
- IOH、IOL




Test circuit 3 schematic diagram

## 7.4 TEST CIRCUIT 4

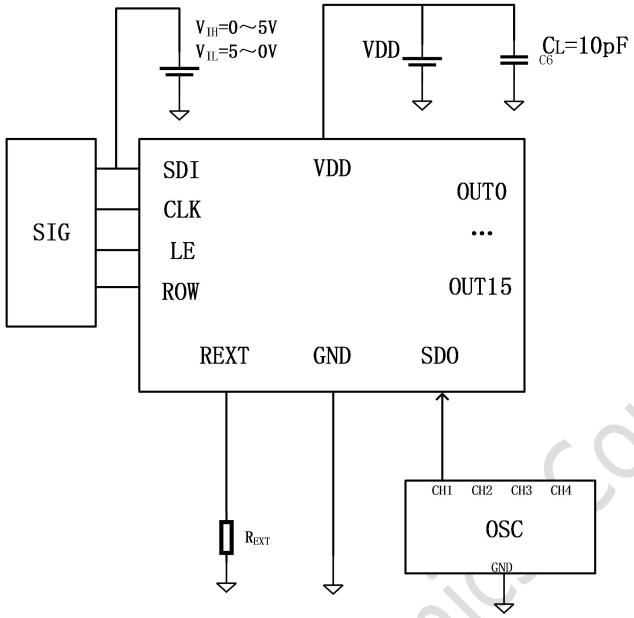
- VOH、VOL




Test circuit 4 schematic diagram

## 7.5 TEST CIRCUIT 5

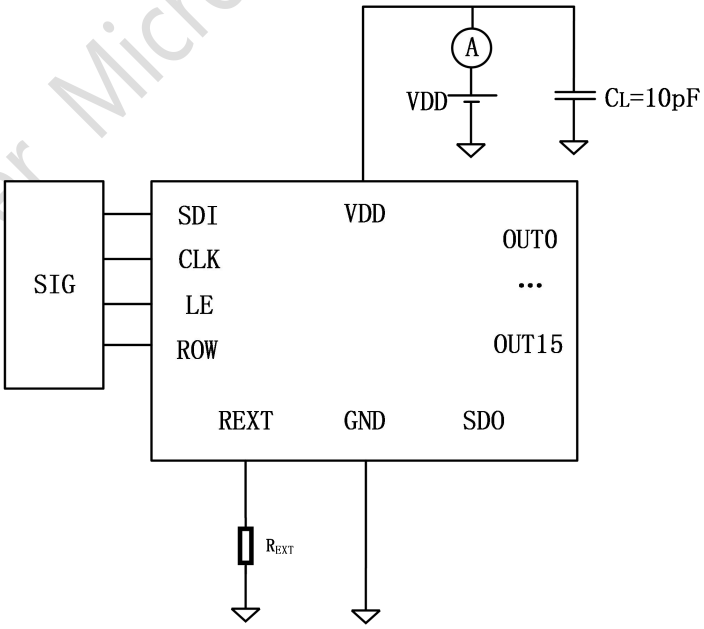
- VIH、VIL




Test circuit 5 schematic diagram

## 7.6 TEST CIRCUIT 6

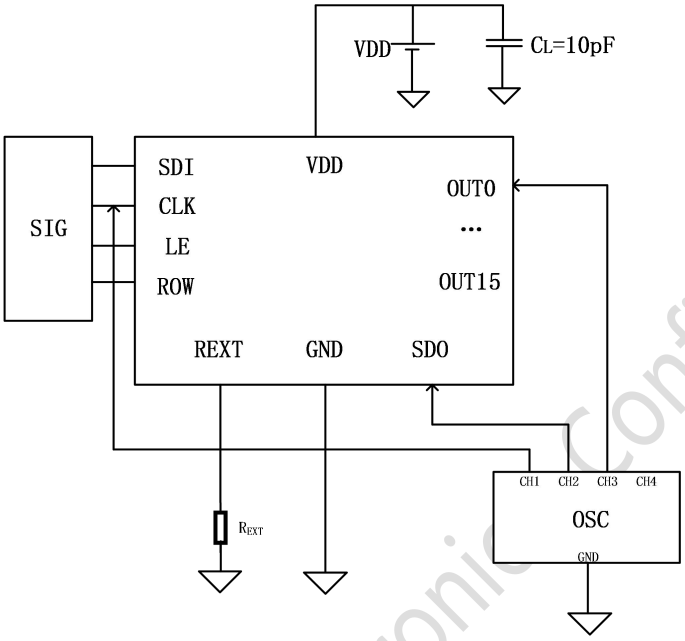
- Supply Current




Test circuit 6 schematic diagram

## 7.7 TEST CIRCUIT 7

- Dynamic Characteristic



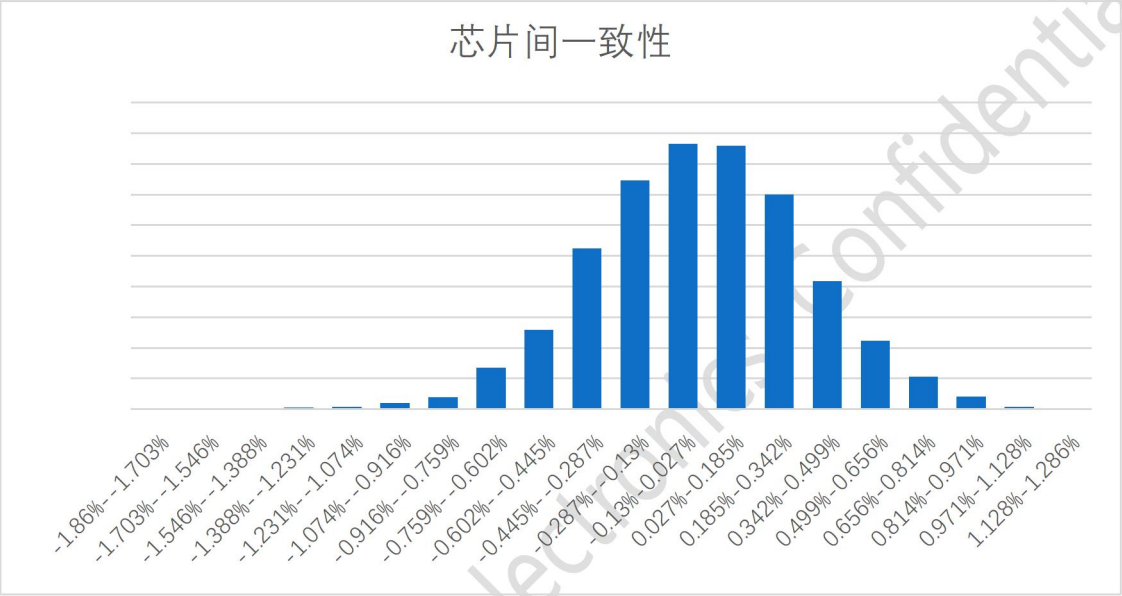

Test circuit 7 schematic diagram

# 8 TYPICAL CHARACTERISTIC DIAGRAM

## 8.1 CONSTANT CURRENT SOURCE ACCURACY TEST CHART

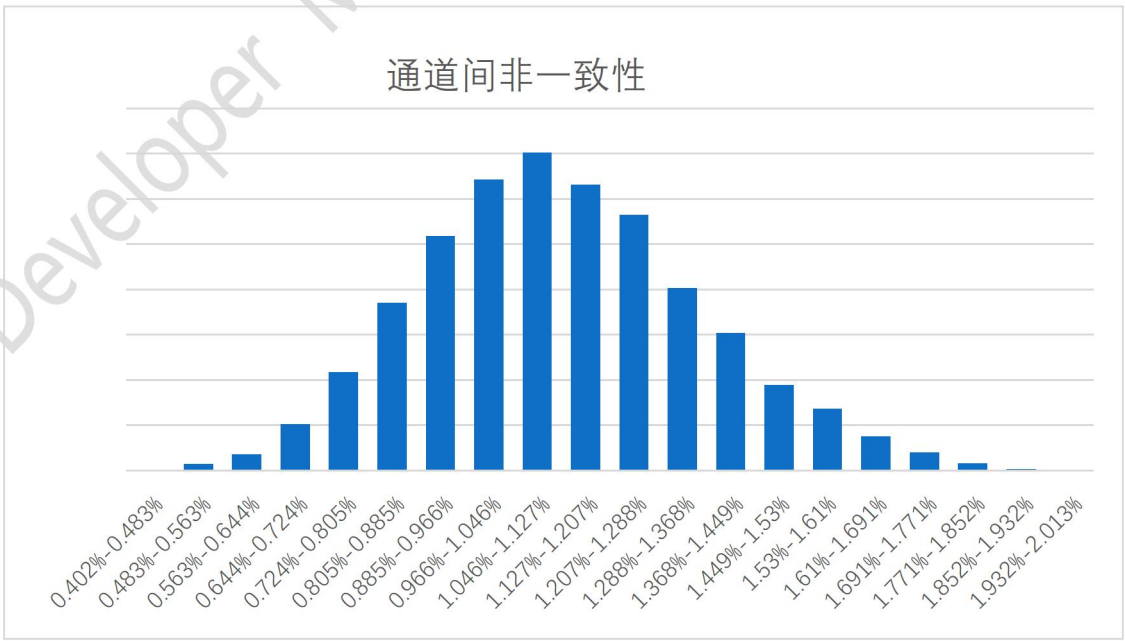
### 8.1.1 INTER-CHIP CURRENT ERROR

Inter-channel current error=$\frac{\text{Average channel current} - \text{average of all chip channels}}{\text{Average of all chip channels}}$




### 8.1.2 INTER- CHANNEL CURRENT ERROR

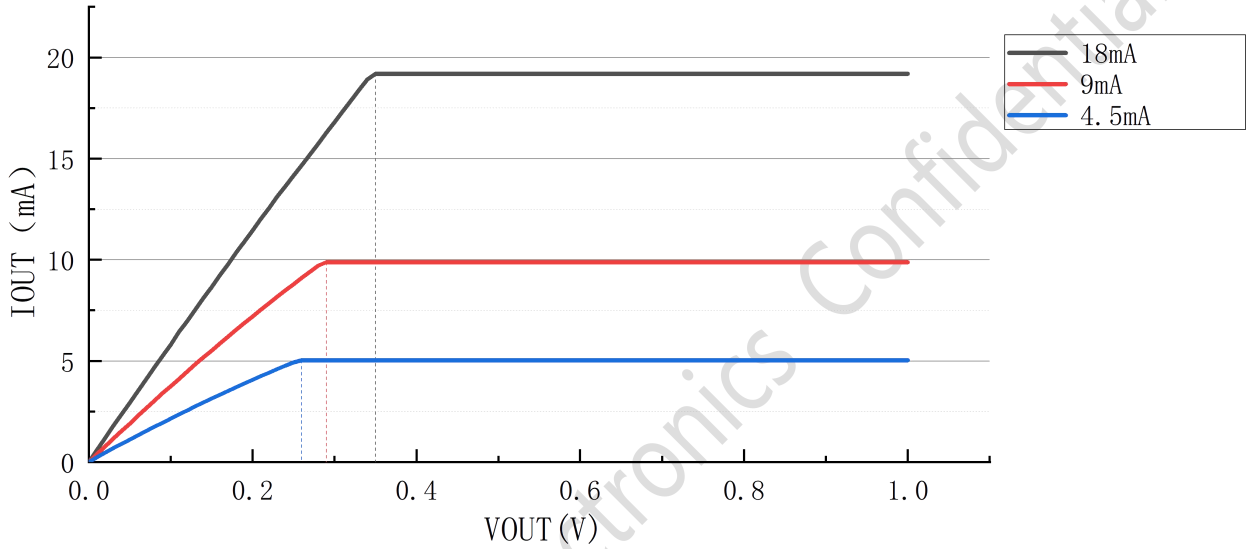
Current error between channels =$\frac{\text{Imax}-\text{Imin}}{\text{Imax}+\text{Imin}}$



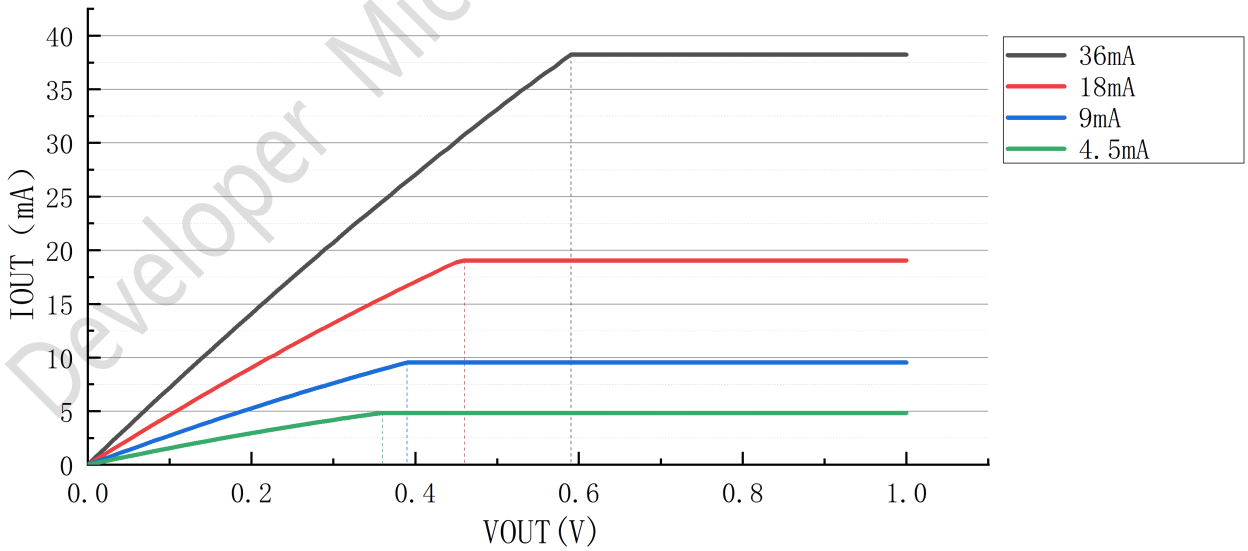
## 8.2 CONSTANT CURRENT SOURCE INFLEXION POINT

When the DP3252 is applied to the design of LED displays, the current differences between channels and even between chips are minimal. This is due to the DP3252's excellent constant current output characteristics::

- The maximum on-chip channel current is less than ±2.5%, and the maximum on-chip current error is less than ±2.0%;
- When the load terminal voltage (Vout) changes, the stability of the output current is not affected, as shown in the figure below:




The relationship between IOUT and VOUT when VDD=2.6V-5.5V is low transition



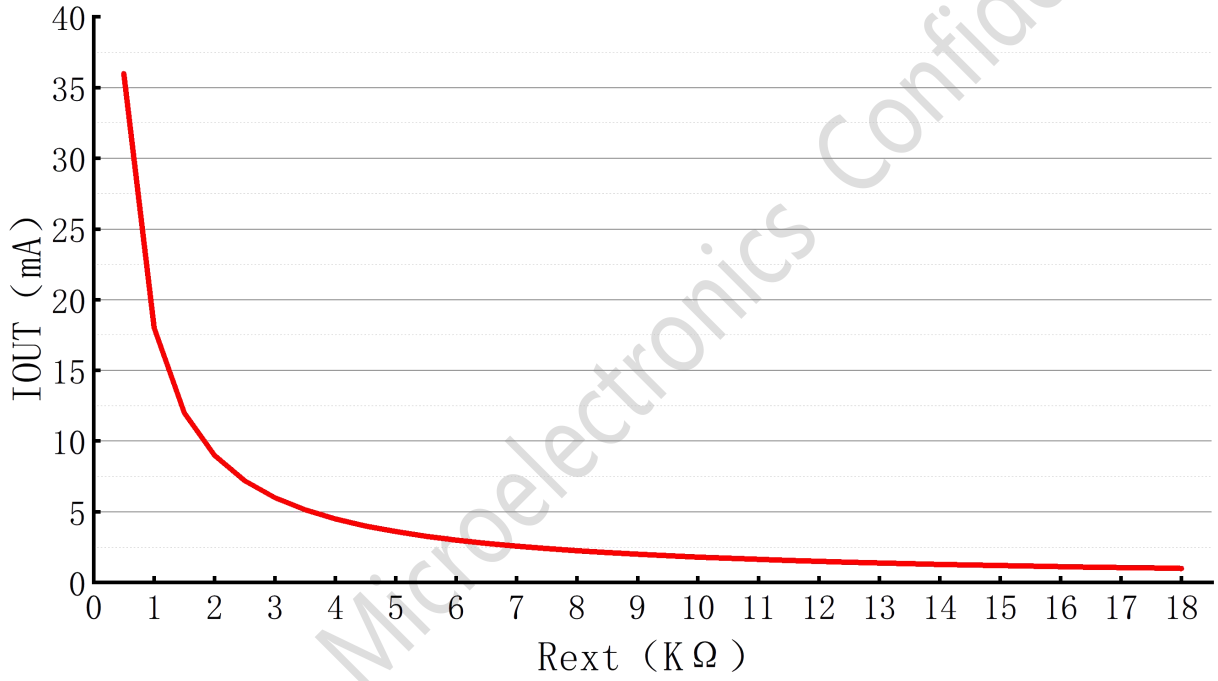

The relationship between IOUT and VOUT when VDD=2.6V-5.5V is not low transition

## 8.3 ADJUST OUTPUT CURRENT BY AN EXTERNAL RESISTOR

Output current value is calculated by the following formula:

$$\mathbf{IOUT} = \frac{IGAIN*18}{Rext}\mathbf{,\ 20\% \le IGAIN \le 200\%}$$

The REXT in the formula is the resistance to the ground of the chip's 23PIN REXT port. For example, when the current gain IGAIN=100%, REXT=1kΩ, the output current value can be obtained by calculating the formula 18mA.




IGAIN=100%, the relationship between REXT and Iout

## 8.4 RESISTIVE-FREE MODEL WITH CURRENT ADJUSTED BY REGISTER

Output current value is calculated by the following formula:

Iout=[70uA+0.4uA*(reg0x0f<6:0>-16)]*reg0x08<7:0>*(1+0.5*reg0x0b<5>)

# 9 TYPICAL DISPLAY EFFECT SAMPLE IMAGE

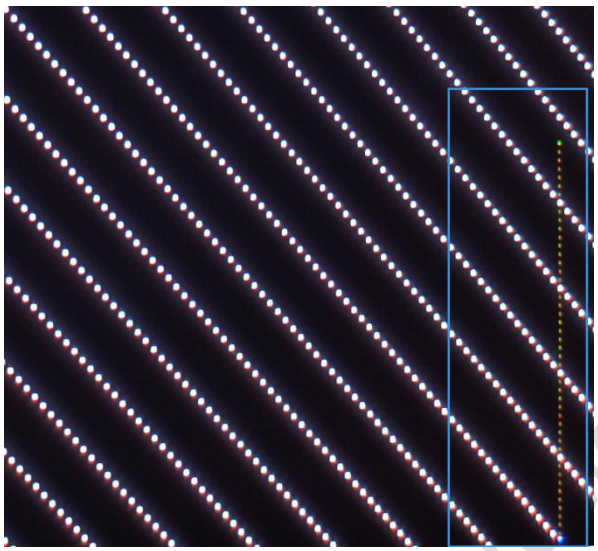
- The specific display effect will be affected by the conditions of the lamp board and register parameters. The following test results are for reference only.

## 9.1 DISPLAY EFFECT

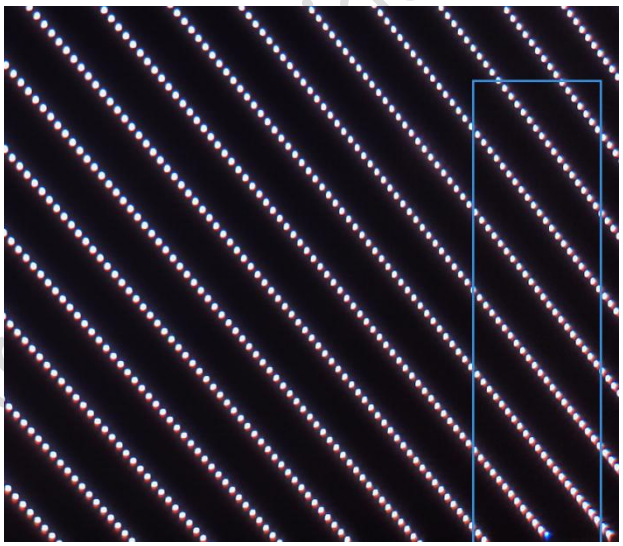
### 9.1.1 REMOVE OPEN CIRCUIT BAD SPOT CROSSES

The following is a comparison of the display effect before and after removing the open circuit bad spot cross, you can see:

- Chip can remove the bad cross well after removing the open bad cross function, optimize the display effect.



Display Effect before Removing open circuit bad spots cross

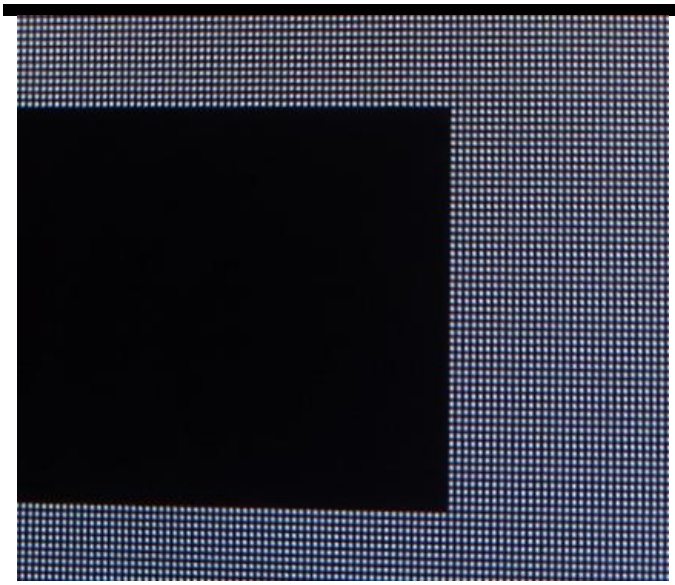


Display effect after removing the open circuit bad spot cross

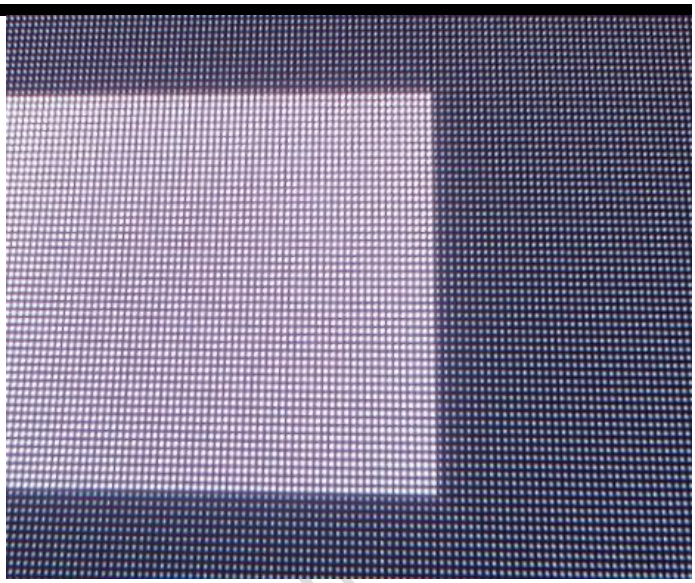
### 9.1.2 HIGH AND LOW GRAY INTERFERENCE AND COUPLING DISPLAY BAD EFFECT OPTIMIZATION

The following figure is the optimization effect of high-low gray interference and coupling display poor effects can be seen:

- The low gray coupling of the block and the low gray coupling of the white block are not sensed.
- Chip show good display effect.



黑块低灰耦合测试显示效果

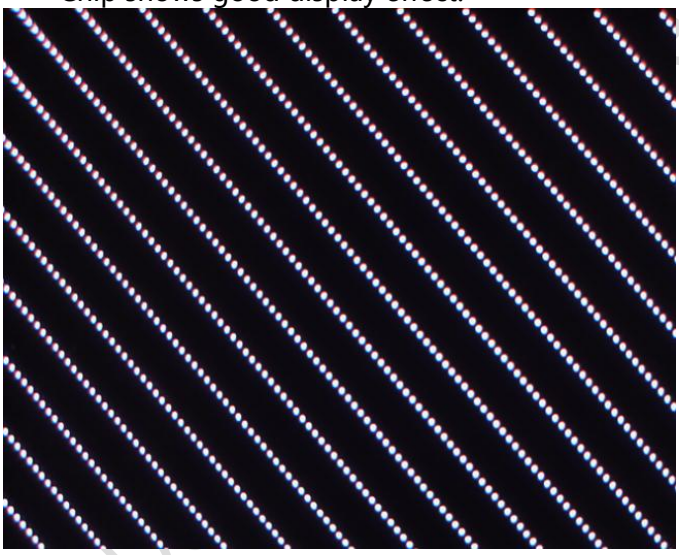


白块低灰耦合测试显示效果

### 9.1.3 REMOVE GHOSTINESS AND BANDLESS LIGHTING EFFECTS

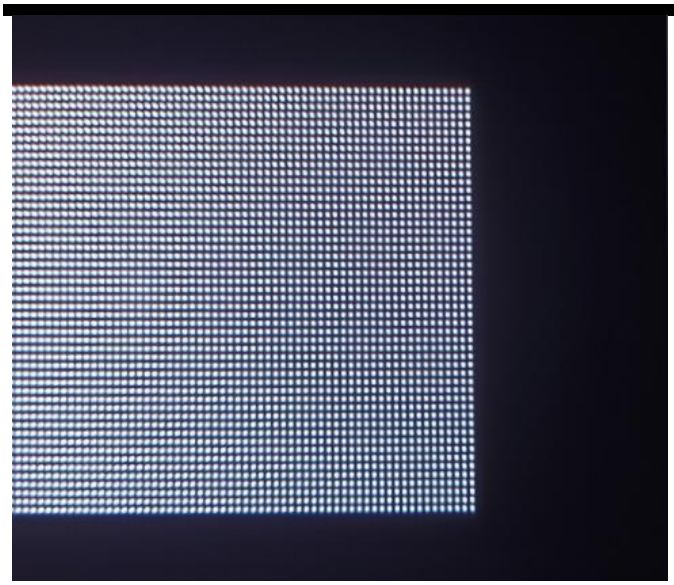
Below is the removal of ghosting and bandless lighting effect that can be seen:

- Oblique scanning ghost, text ghost and other problems cannot be observed.
- Highlight block with bright, oblique scan superimposed highlight block with bright test results are very good.
- Chip shows good display effect.

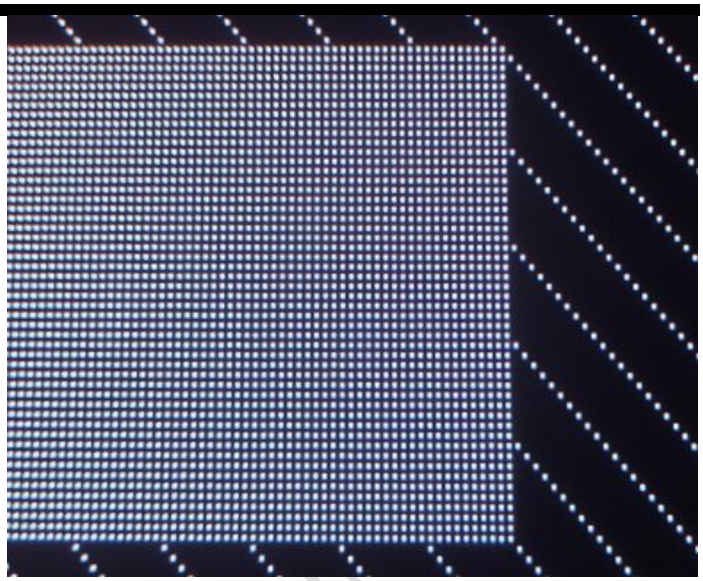


Slanted scan ghosting test display effect

Text ghosting test display effect



Highlight block with light test display effect



Oblique scan superimposed highlight block with light test display effect

# 10 INSTRUCTION AND REGISTER

## 10.1 REGISTER INSTRUCTION

| Instruction Name | LE | Description |
|---|---|---|
| DATA_LATCH | 1 | Latch 16bit data to SRAM |
| DDR | 2 | Enter Double-edge Mode |
| VSYNC | 3 | Update Display Data |
| WR_CFG | 5 | Write Register |
| PRE_ACT | 14 | Write Enable |
| SDR | 15 | Enter Single-edge Mode |

## 10.2 DATA INSTRUCTIONS

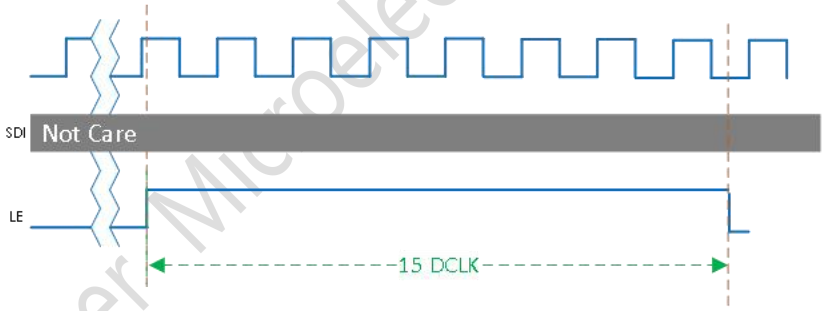
| Data sending Sequence | Line | Channel |
|---|---|---|
| **1** | **Line 0** | **Channel 15 (OUT15)** |
| **2** | | **Channel 14 (OUT14)** |
| **……** | | **……** |
| **16** | | **Channel 0 (OUT0)** |

| | | |
|---|---|---|
| 17 | Line 1 | Channel 15 (OUT15) |
| 18 | | Channel 14 (OUT14) |
| ..... | | ..... |
| 32 | | Channel 0 (OUT0) |
| ..... | | |
| 497 | Line 15 | Channel 15 (OUT15) |
| 498 | | Channel 14 (OUT14) |
| ..... | | ..... |
| 512 | | Channel 0 (OUT0) |

## 10.3 SINGLE/DOUBLE MODE SWITCH

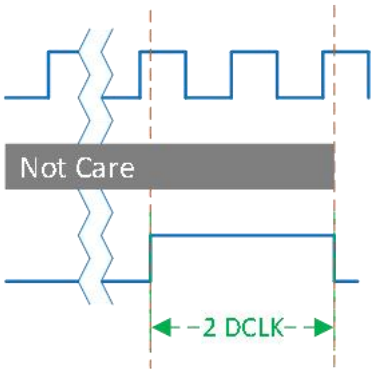
1. Sample SDI data with CLK rising edge in single edge mode, and sample SDI data with CLK rising edge and falling edge in double edge mode.
2. CLK rising edge counting is used for fixed OE signal width
3. The command for single-mode and dual-mode along mode switchover needs to be sent once after it is powered on

To enter the single-edge mode after power-on, send the command shown in the following figure:




15 DCLK edges (up + down) are set to SDR

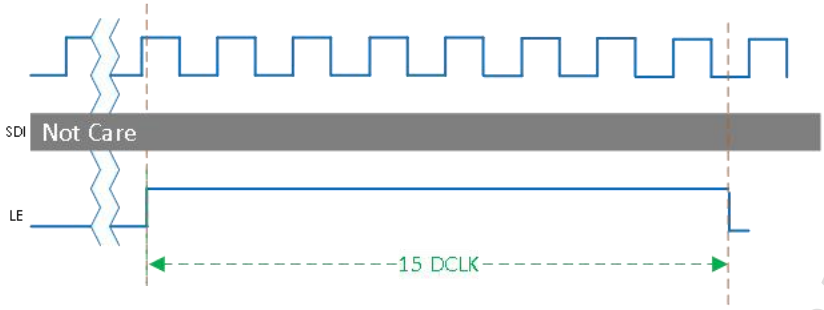
To enter the dual-edge mode after power-on, send the command shown in the following figure




The two DCLK rising edges are set to DDR

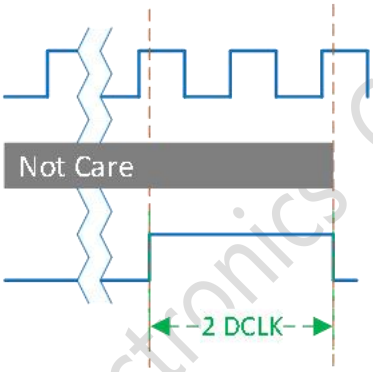
If the customer needs to adjust the single and double edges during debugging

If already in dual edge mode and need to enter single edge mode, send the following command




In double edge mode, 15 DCLK edges (up + down) are set to SDR

If already in single edge mode, you need to enter double edge mode




In single-edge mode, the two DCLK rising edges are set to DDR

## 10.4 WRITE REGISTER

Send PRE_ACT first, then run WR_CFG, LE is 5 DCLK width, the first input 8bit is the register address bit, the last input 8bit is the data bit of the corresponding register address。

For example：

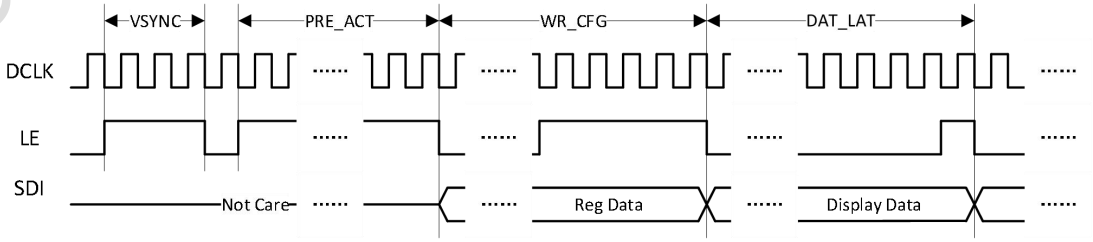
{A7, A6, A5, A4, A3, A2, A1, A0} = 8’ b0000_0111;

{D7, D6, D5, D4, D3, D2, D1, D0}=8’ b1001_1101;

That is, register 0x07 (8 'b0000_0111) is set to 8' b1001_1101.

## 10.5 REGISTER SINGAL SENDING WAY

The specific driving methods are as follows：




As shown in the figure above, the order of sending instructions and data in each frame：

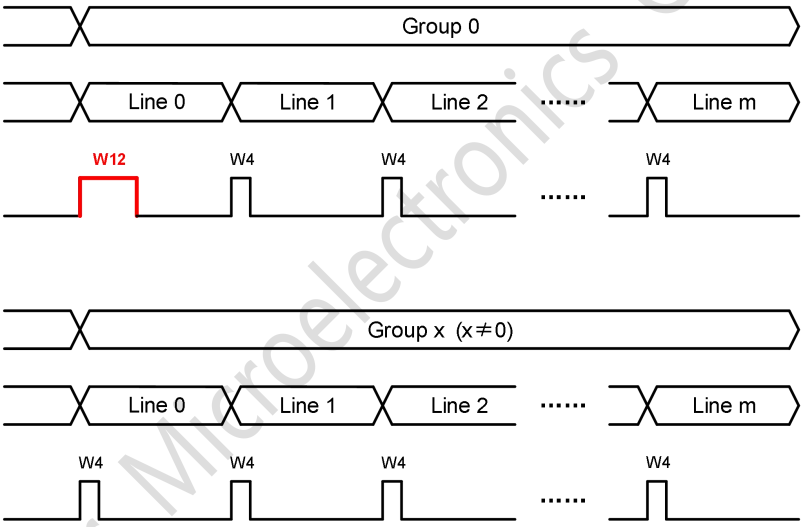
1. Send VSYNC。
2. Send PRE_ACT。
3. Send WR_CFG and write the register configuration. Each frame can only write a register value of one address, and 15 frames complete the refresh of all registers (a total of 15 valid register addresses) to save configuration time.
4. Send DAT_LAT several times to write display data together with SDI.

5. The data sending bit is displayed as 16 bits.

## 10.6 ROW SIGNAL SENDING WAY

The DP3252 integrated on-chip GCLK generation circuit changes the OE signal of the universal constant current chip to the ROW signal, using ROW the rising edge of the ROW represents the beginning of a row display, where the high level width of the row has two types, namely:

1.W12: The high-level width of the ROW is 12 DCLK width
2.W4: The high-level width of the ROW is 4 DCLK width



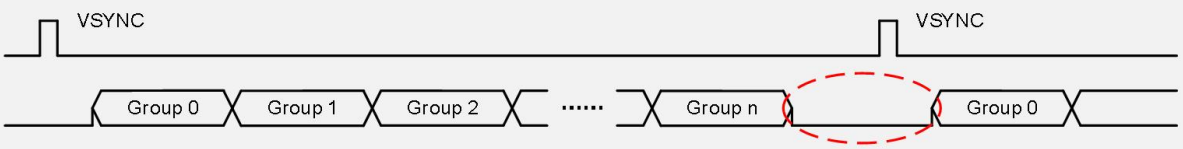

As shown in the figure above, when ROW signals are sent, only the first ROW of Group 1 (Line 0) needs to send ROW signals of W12, and other ROW signals are sent according to W4.

## 10.7 PWM DISPLAY MODE

DP3252 integrated four PWM display modes:

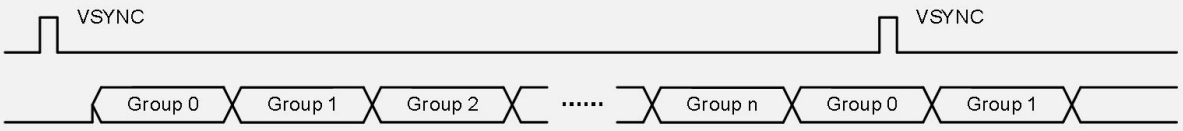
1. General frame synchronization mode; 2. High-gray data independent refresh synchronous mode;
3. High-gray data independently refreshes asynchronous mode; 4. Low Ash High Brush mode

### 1. 通用帧同步模式



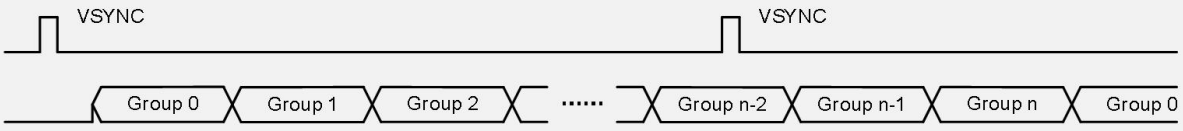

显示组数为控制卡自动配置
组数（取整）=帧周期/一组的显示时间
一组的显示时间=一行的显示时间*扫描行数
一行的显示时间-换行时间=(2*(reg0x05[7:4]+1)+2*(reg0x05[3:0]+1)+4*(reg0x04[6:0]+1))/(reg0x06[2:0]+1)个DCLK

### 2. 高灰度独立刷新同步模式



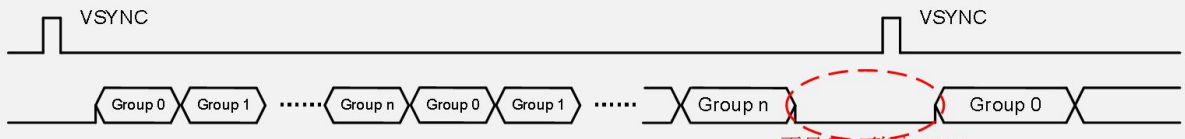

显示组数为控制卡自动配置
组数（取整）=帧周期/一组的显示时间
一组的显示时间=一行的显示时间*扫描行数
一行的显示时间-换行时间=(2*(reg0x05[7:4]+1)+2*(reg0x05[3:0]+1)+4*(reg0x04[6:0]+1))/(reg0x06[2:0]+1)个DCLK

### 3. 高灰度独立刷新异步模式




显示组数为手动配置（默认配置为64组）
一组的显示时间=一行的显示时间*扫描行数
一行的显示时间=(2*(reg0x05[7:4]+1)+2*(reg0x05[3:0]+1)+4*(reg0x04[6:0]+1))/(reg0x06[2:0]+1)+换行时间

### 4. 低灰高刷模式




一行的显示时间=(2*(reg0x05[7:4]+1)+2*(reg0x05[3:0]+1)+4*(reg0x04[6:0]+1))/(reg0x06[2:0]+1)+换行时间
一组的显示时间=一行的显示时间*扫描行数
显示组数为手动配置（默认配置为64组）所有组的显示时间=一组的显示时间*显示组数
高刷倍率（取整）=帧周期/所有组的显示时间
两个Vsync之前需要发送高刷倍率*显示组数*扫数个ROW信号（上图以两倍高刷为例）

### 10.7.1 GENERAL FRAME SYNCHRONIZATION MODE

Working mode and related configurations as follow:

1. Configure REG0X0C [7:6] = 0 and set the PWM display mode to Universal Frame Sync Mode
2. The number of DCLK per line is calculated using the Formula
3. The configuration shows the number of data sets, REG0X03[6:0] = refresh rate/frame rate -1(if refresh rate is not equal to 3840 or 7680, use Depp's gamma DLL)
4. After VSYNC, the first Line (Line 0) of Group 1(Group 0)
5. Stop displaying data from the current frame until the next VSYNC comes

### 10.7.2 HIGH GRAY DATA REFRESH FRAME SYNCHRONIZATION MODEL INDEPENDENTLY

Working mode and related configurations as follow:

11. Configure REG0X0C [7:6] = 2, set PWM display mode to high gray data independent refresh frame synchronization mode under this mode display refresh rate support 3840HZ ~ 7680HZ, configure display data group register reg0x03[6:0] = 127
2. Calculate a set of display times = frame period/(refresh rate/frame rate)
3. Calculate the display time of a row = a set of display times/number of rows
4. The DCLK number of each row is calculated according to the formula, and the formula is satisfied by adjusting the row gray level series, the DCLK frequency and the register reg0x6[1:0] .
5. Row is sent continuously at a fixed display frequency. The frequency of the ROW is independent of VSYNC the frequency of the ROW signal = 1/1 ROW display time = 1/2 time between the rising edges of the ROW
6. Row 0 of group 0 sends the ROW signal of W12, other cases send the ROW signal of W4 every (group number * ROW scan number-RRB- ROW signal, only W12 W12, and in this way has been circulating.
7. If the refresh rate is not equal to 3840 or 7680, you need to use Depp's gamma dll 。

### 10.7.3 HIGH-GRAY DATA INDEPENDENTLY REFRESHES ASYNCHRONOUS MODE

Working mode and related configurations as follow:

1. Configure REG0X0C [7:6] = 3, set the PWM display mode to high gray data independent refresh asynchronous mode
2. The number of DCLKS per line is calculated using the Formula
   Displays the number of data groups manually configured, the default is 64 groups (reg0x03[6:0] = 7' H3F).

3. ROW continuously transmission at a fixed display frequency without interruption, and ROW frequency is independent of VSYNC.

Row signal frequency = 1/1 ROW display time = 1/2 ROW rise edge time

4. Row 0 of group 0 sends the ROW signal of W12, other cases send the ROW signal of W4 per (group number (as per register configuration value) * ROW scan number-**RRB-** ROW signal, only W12, and in this way has been circulating. There is no limit to the number of cycles allowed in a frame.
5. Visual refresh rate = 1/( one line display time * scans)

### 10.7.4 LOW GRAY HIGH BRUCH MODE

Working mode and related configurations as follow:

1. Configure REG0X0C [7:6] = 1, set PWM display mode to Low Ash High Brush Mode
2. Display the number of groups manually (the default is 64) . If the refresh rate is not equal to 3840 or 7680, use Depp's gamma DLL
3. The DCLK number of each row is calculated according to the formula, and the display time of a row is calculated
4. Calculate a set of display times = one line of display times * number of lines
5. Calculate all group display times = one group display times * number of groups
6. High brush rate (rounded) = frame period/display time for all groups
7. Before both VSYNC need to send a high brush rate * display array number * scan several ROW signals
8. After VSYNC, Line 1(Line 0) of Group 1(Group 0)
9. The data for the current frame is displayed at a high brush rate and then stopped until the next VSYNC arrival.
10. Visual refresh rate = frame rate * data set * high refresh rate = (3840/7680 Hz) * high refresh rate 11. The low-gray high-brush mode only needs to change the ROW signal according to the above steps, the gray level does not need to be adjusted.

## 10.8 RELEVANT CONFIGURATION OF PWM DISPLAY

### 10.8.1 NUMBER OF ROW SCANS CONFIGURED

DP3252 supports up to 32 line scans, configured as REG0X02[5:0] = number of line scans -1

### 10.8.2

Reg0x04[6:0] represents a row of PWM display length, one row of PWM display length = 4 * (reg0x04[6:0] + 1), maximum support 128x4 = 512 if the configuration row gray level is 128, then set reg0x04[6:0] = 7' H1F = 31

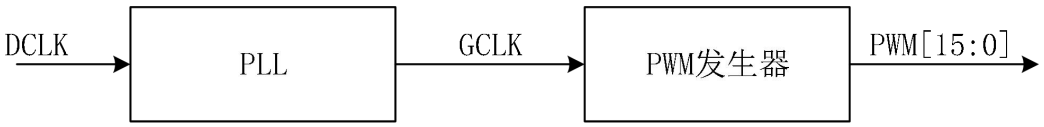
### 10.8.3 PWM DISPLAY PACKET CONFIGURATION

Reg0x03[6:0] represents the number of PWM groups, PWM shows the number of groups = Reg0x03[6:0] + 1, the maximum number of support groups is 128 groups

In frame synchronous mode, PWM display group number = refresh rate/frame rate, configure reg0x03[6:0] = refresh rate/frame rate -1

In asynchronous mode, the PWM display packet can be configured independently (independent of the refresh rate)

## 10.8.4 INTERNAL GRAYSCALE CLOCK CONFIGURATION




DP3252 integrates PLL on chip to produce gray clock GCLK.
The relevant calculation formula is as follows:
FGCLK=FDCLK*(reg0x06[1:0] +1)

## 10.8.5 PWM GRAYSCALES SERIES & GAMMA GENERATION

PWM gray-scale series (maximum) = * PWM gray-scale series show grouping = 4 * (reg0x04 [lost] + 1) * (reg0x03 [lost] + 1) - 1

reg0x04[6:0]=7’ h7f, reg0x03[6:0]= 7’ h7f

PWM gray level (maximum)=4*(127+1)*(127+1)-1=65535=16bit

Gamma can be calculated and generated according to the PWM gray level (maximum) (this part is generated by the control card manufacturer according to their own gamma generation formula)

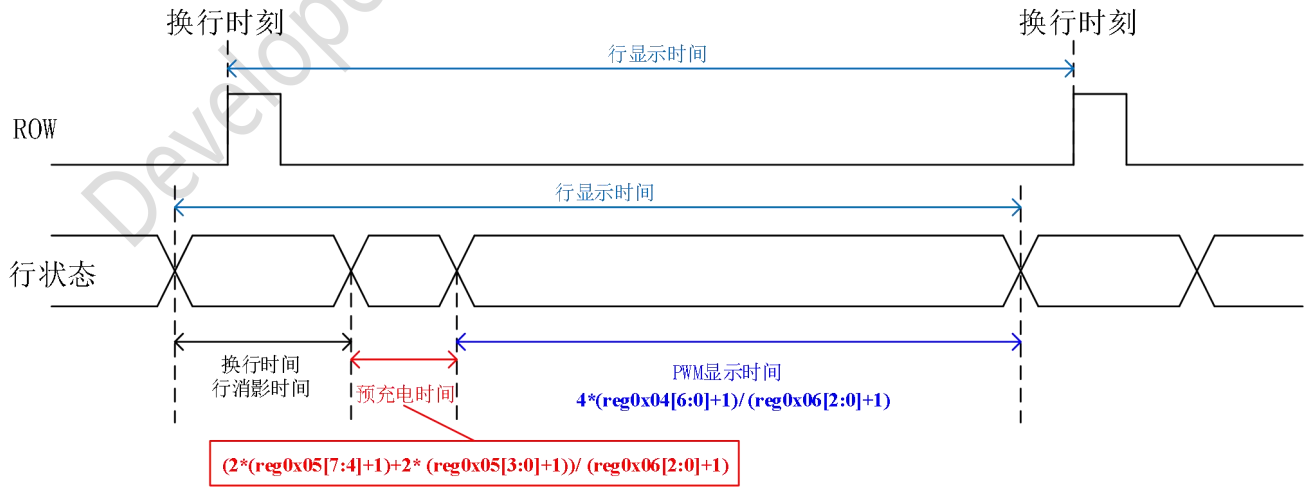
The maximum chip gray level only supports 16bit (low 16 bits are valid).

## 10.8.6 CALCULATED THE DISPLAY TIME FOR EACH ROW

The display time of each line is expressed by the number of DCLK, and the calculation formula is as follow:

**(2*(**reg0x05**[7:4] +1) +2*(**reg0x05**[3:0] +1) +4*(**reg0x04**[6:0] +1))/(**reg0x06**[2:0] +1)** + break time

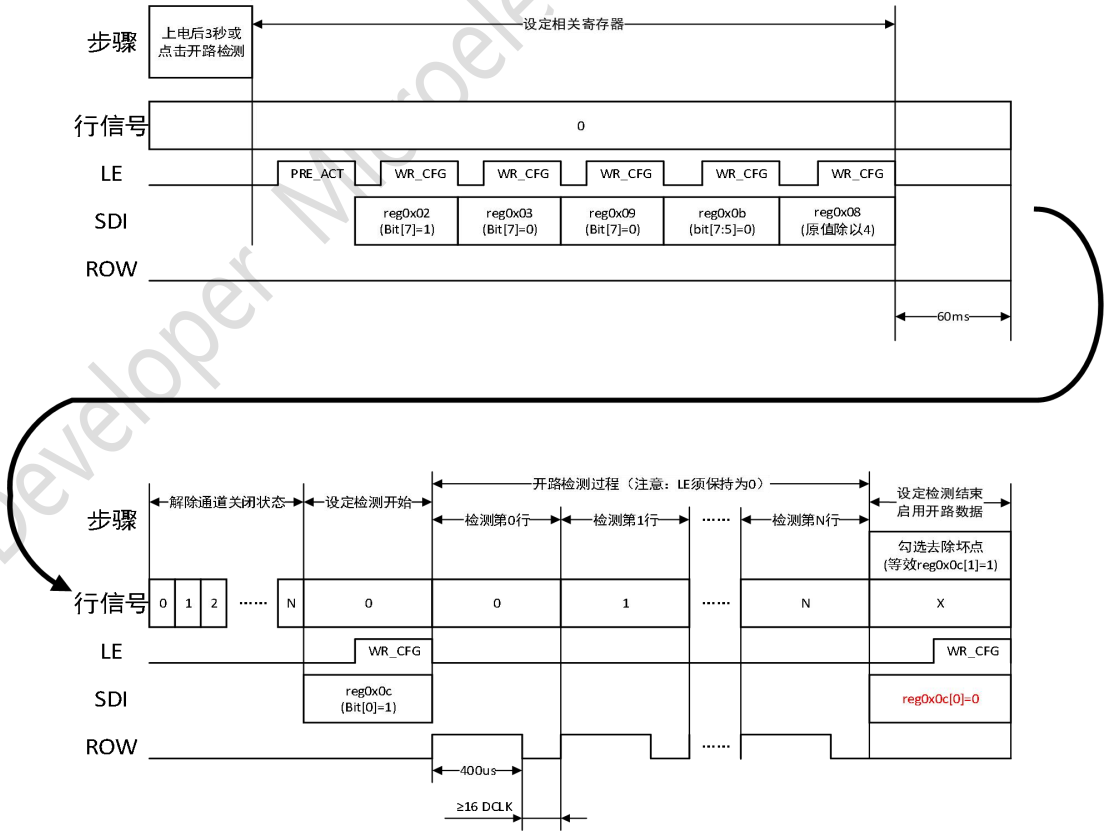
Note: the above results are rounded.



## 10.9 OPEN CIRCUIT DETECTION AND REMOVAL OF BAD SPOTS

Selected【**Remove bad spots**】: reg0x0c[1]=1 ;
Non-selected【**Remove bad spots**】: reg0x0c[1]=0
Open circuit detection timing:

1.The open circuit test is performed 3 seconds after power-on or after clicking open circuit test.
2. Configure reg0x02[7]=1, reg0x03[7]=0 (Enable Open detection mode)
Configure reg0x0b[7:5]=0 (Set constant current inflection point to the lowest)
Configure reg0x08[7:0] move two digits to the right and fill the high position with 0, (configure output current to 25% of normal)
3.Line signal switch to line 0 and stop all line signals for one frame time (60ms)
4. Change the line signal, quickly scan from line 0 to the last line, and then back to line 0 (this step is mainly to avoid the closure of the output channel that exists in some line driver chips).
5. Configure reg0x0c[0]=1 (Open detection mode is enabled)
6. Sending a Row signal, set the Row to high first and then to low. The high level time (400us recommended) is the time required for detecting a ROW, and the low level time (≥16 DCLK recommended) is the data collection and latch time.
7. Line feed, as many lines as need to be scanned, step 6 perform as many times. Line breaks are recommended to align with the rising edge of the ROW..
8. After the detection is complete, configure reg0x0c[0]=0 (Turn off open detection mode), reg0x0c[1]=1 (selected【**Remove bad spots**】)。
9. During open-circuit detection, LE=0, DCLK is normally transmitted continuously (at least 128 DCLK between two rows are guaranteed).



## 10.10 REGISTER

| Register | Register Function Name | Register function description & default value |
|---|---|---|
| 0x02 | | R：2A G：2A B：2A |
| 7 | OPDET_EN_A1 | OPDET_EN_A1 High effective; It must work with OPDET_EN_A2 and OPDET_EN_A3 |
| 6 | | Reserved |
| 5:0 | LINE_SET<5:0> | Scanning Lines= LINE_SET +1 |
| 0x03 | | R：3F G：3F B：3F |
| 7 | OPDET_EN_A2 | OPDET_EN_A2 is low valid. It must work with OPDET_EN_A1 and OPDET_EN_A3 |
| 6:0 | GROUP_SET<6:0> | Display refresh ratio =REG03<6:0>+1 |
| 0x04 | | R：20 G：20 B：20 |
| 7 | | Reserved |
| 6:0 | PWM_WIDTH<6:0> | Row GCLK number |
| 0x05 | | R：34 G：34 B：34 |
| 7:3 | DISSHD_TIME_1<3:0> | Shadow elimination Time -0 to 15, total16 levels, the default value is 0 |
| 2:0 | DISSHD_TIME_2<3:0> | Shadow elimination time -0 ~15, total 16 levels |
| 0x06 | | R：42 G：42 B：42 |
| 7:3 | DECOUP_RAT<4:0> | Coupling optimization coefficient |
| 2:0 | PLL_DIV<2:0> | GCLK frequency doubling<br>0：1 frequency doubling<br>1：2 frequency doubling<br>2：3 frequency doubling<br>3：4 frequency doubling |
| 0x07 | | R：00 G：00 B：00 |
| 7 | Gamma_COARSE_EN | Gamma Coarse switch -1: coarse switch enabled 0: coarse switch off |
| 6:4 | Gamma_COARSE<2:0> | Gamma 粗调等级-0~7 级，共 8 级 |
| 3 | Gamma_FINE_EN | Gamma fine-tune switch -1: fine-tune enabled 0: fine-tune disabled |
| 2:0 | Gamma_FINE<2:0> | Gamma Fine level -0 to 7, 8 in total |
| 0x08 | | R：7F G：7F B：7F |
| 7:0 | IGAIN<7:0> | reg08[7:6] is a progression of 50% of the current gain<br>reg08[5:0]= round (128*IGAIN/(reg08[7:6]+1))-1 |
| 0x09 | | R：60 G：60 B：60 |
| 7 | EN_IR | 0：resistance 1：non-resistance |
| 6:5 | | Reserved |
| 4:0 | DECOUP_1<4:0> | Coupling optimization level 1-0 ~31，total 32 levels |
| 0x0a | | R：BE G：BE B：BE |
| 7:6 | DECOUP_ENHANCE<1:0> | Coupling optimization enhancement level - decreases from 0 to 3 |
| 5 | | Reserved |

| | | |
|---|---|---|
| 4 | DISSHD_EN | Extinction level switch - On :1 Off: 0 |
| 3 | DECOUP_EN | Coupling optimization switch |
| 2:1 | PIT_OPT<1:0> | Low grey pitting optimization -0 ~3, total 4 levels, the default is level 3 |
| 0 | LG_ENHANCE | Low gray display effect enhancement switch |
| 0x0b | | R：28 G：30 B：31 |
| 7:5 | CORNER <2:0> | Constant current output inflection point level<br>0: low inflection point (0.18 V - 0.3 V) corresponds to the current range of 0.5mA~18mA<br>1：Non- low inflection point (0.3 V - 0.45 V) corresponds to the current range of 0.5mA~25mA |
| 4:0 | DISSHD_LEVEL<4:0> | Shadow Elimination level，0~31 level，total 32 levels |
| 0x0c | | R：90 G：90 B：90 |
| 7:6 | SYNC_MODE<1:0> | 0：frame synchronization mode<br>1：Low gray high brush model<br>2：High gray data independently refreshed in synchronization model<br>3：High gray data independently refreshed in asynchronous mode |
| 5:4 | LP_MODE<1:0> | Energy-saving model<br>0：Dynamic energy saving<br>1：Dynamic Energy saving + Black screen energy saving mode 1-Performance is preferred<br>2：Dynamic Energy Saving + Black screen Energy Saving mode 2-Low power consumption is preferred<br>3：Dynamic Energy Saving + Black Screen Energy Saving Mode 3-Extremely low power consumption |
| 3:2 | | Reserved |
| 1 | RM_OP | Remove the bad spot function switch |
| 0 | OPDET_EN | If both OPDET_EN_A1 and OPDET_EN_A2 are met, OPDET_EN is enabled to enter the open detection mode |
| 0x0d | | R：08 G：12 B：18 |
| 7:5 | | Reserved |
| 4:0 | DECOUP_LEVEL<4:0> | Coupling optimization level, 0 ~31, total 32 levels |
| 0x0e | | R：00 G：00 B：00 |
| 7:6 | | Reserved |
| 5 | PRECHA_EN | Enable coupling Optimization 2 |
| 4:0 | VS_PRECHA | Coupling optimization level 2-0 ~31, total 32 levels |
| 0x0f | | R：00 G：00 B：00 |
| 7 | | Reserved |
| 6:0 | IGAINL | 'Resistance-free current regulation range +/-7.5%, step length 0.5% |
| 0x10 | | R：00 G：00 B：00 |
| 7:0 | | Reserved |

| | | |
|---|---|---|
| 0x11 | | R：00 G：00 B：00 |
| 7 | OPEN_EN_B | Enable coupling optimization 1 |
| 6:0 | | Reserved |
| 0x12 | | R：00 G：00 B：00 |
| 7:0 | | Reserved |
| 0x13 | | R：00 G：00 B：00 |
| 7:0 | | Reserved |
| 0x14 | | R：00 G：00 B：00 |
| 7:0 | | Reserved |
| 0x15 | | R：00 G：00 B：00 |
| 7:0 | | Reserved |
| 0x16 | | R：00 G：00 B：00 |
| 7:0 | | Reserved |
| 0x17 | | R：00 G：00 B：00 |
| 7:0 | | Reserved |

# 11 ENCAPSULATION COOLING POWER ($P_D$)

The maximum heat dissipation power of the encapsulation is determined by the formula: $P_{D(\max)} = \frac{(T_j - T_a)}{R_{th(j-a)}}$

When all 16 channels are open, the actual power is:

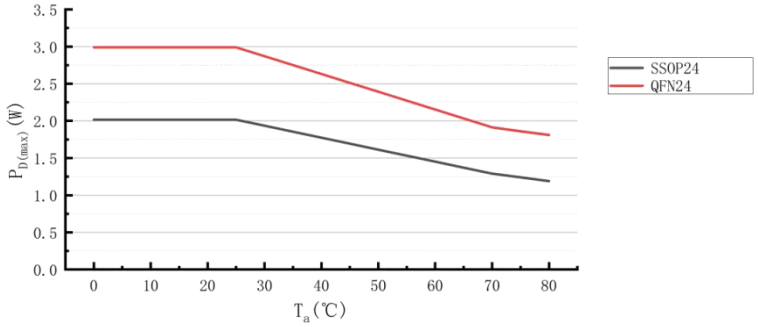
$$P_{D(act)} = I_{DD} * V_{DD} + I_{OUT} * Duty * V_{DS} * 16$$

To ensure that $P_{D(act)} \le P_{D(max)}$ output maximum current and duty cycle relationship is:

$$I_{OUT(\max)} = \frac{\frac{T_j - T_a}{R_{th(j-a)}} - (I_{DD} * V_{DD})}{V_{DS} * Duty * 16}$$

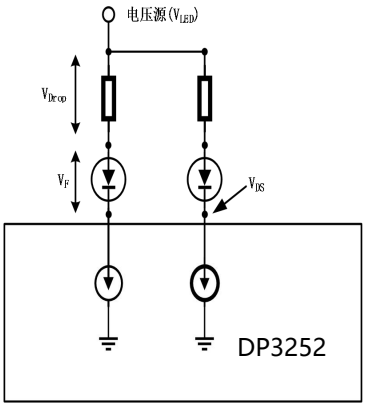
Therein $T_j$ is the junction temperature ($T_j$=150℃), $T_a$ is the ambient temperature, $V_{DS}$ is the constant current output port voltage, Duty is the duty cycle, and $R_{th(j-a)}$ is the thermal resistance of the encapsulation.

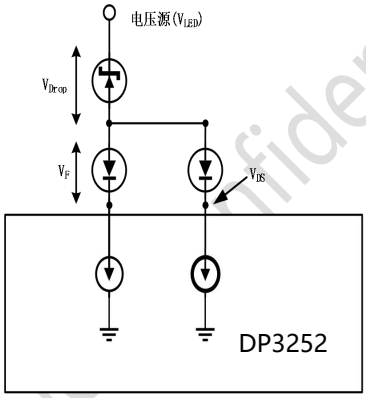
| 封装 | $R_{th(j-a)}$(℃/W) | $P_{D(max)}$(W) |
|---|---|---|
| QSOP24 | 62 | 2.01 |
| QFN24 | 41.8 | 2.99 |



# 12 LOAD TERMINAL VOLTAGE(VLED)

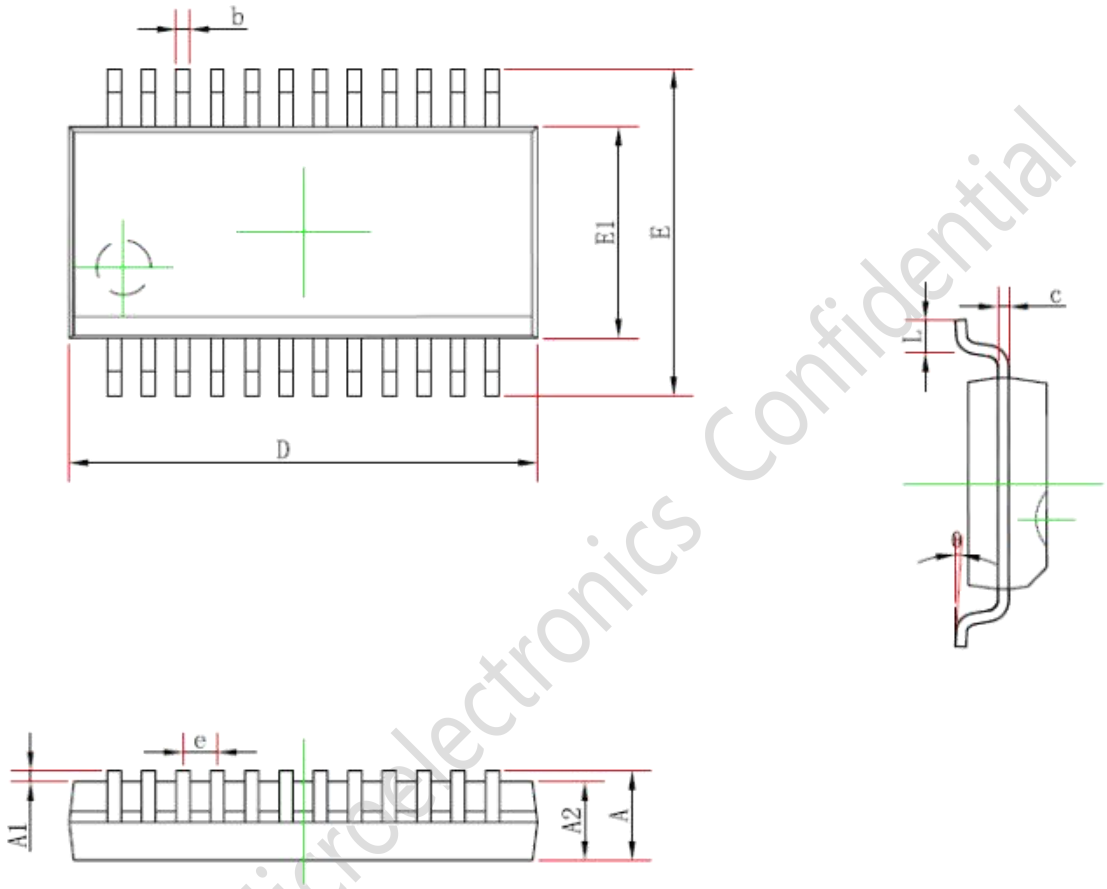
In order to optimize the heat dissipation capacity of the package, it is recommended that the best operating range of the output terminal voltage (VDS) is 0.3V to 1.0V(IOUT= 0.5-36mA). If VDS=VLED-VF and VLED=5V, the high output voltage (VDS) may cause PD (act) > PD (max); In this case, it is recommended to use the lowest possible VLED voltage for use, and an external resistor or voltage regulator can also be used as a VDROP. This results in VDS=(VLED-VF)-VDROP, which reduces the input voltage (VDS) value. The application diagram of the external series resistor or voltage regulator can be referred to the following figure.



# 13 ENCAPSULATION INFORMATION

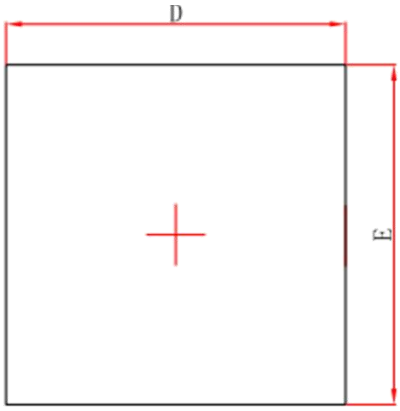
- QSOP24 Plastic Encapsulation Specification Drawing



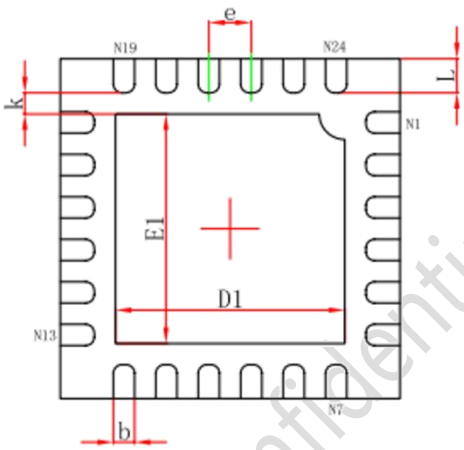



| | Millimeters (mm) | |
|---|---|---|
| | Min | Max |
| A | — | 1.95 |
| A1 | 0.05 | 0.35 |
| A2 | 1.05 | — |
| b | 0.1 | 0.4 |
| c | 0.05 | 0.254 |
| D | 8.2 | 9.2 |
| E1 | 3.6 | 4.2 |
| E | 5.6 | 6.5 |
| e | 0.635TYP | |
| L | 0.3 | 1.5 |
| θ | 0° | 10° |

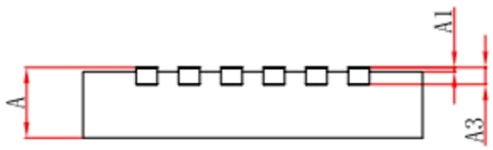
- QFN24 Plastic Encapsulation Specification Drawing




Top View




Bottom View




Side View

| | Millimeters (mm) | |
|---|---|---|
| | Min | Max |
| A | 0.700/0.800 | 0.800/0.900 |
| A1 | 0.000 | 0.050 |
| A3 | 0.203REF | |
| D | 3.924 | 4.076 |
| E | 3.924 | 4.076 |
| D1 | 2.6 | 2.8 |
| E1 | 2.6 | 2.8 |
| k | 0.20MIN | |
| b | 0.200 | 0.300 |
| e | 0.500TYP | |
| L | 0.324 | 0.476 |

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