LED Display Control IC

1 Overview

DP32021 is a serial decoding row driver chip specially designed for LED scanning screens.

DP32021 can completely replace the original 3-8 decoders (74HC138) circuit of LED module (74HC138), and more effectively simplifying the complexity of PCB wiring of LED module, to improve the overall image effect of the display screen.

2 Features

- Working voltage 2.8V~5.5V
- Support arbitrary scans of scanning screen
- PMOS tube of integrated 8-channel power
  - OUT_MAX = 4A @ VDD = 5.0V
  - RON=73mΩ@VDD=5.0V&IOUT=1.0A
- Max power consumption less than 600 mW @ VDD = 5.0V
- Integration of adaptive function of ghosting reduction can effectively eliminate trailing smear
- Ghosting potential configured with register can adapt to more complex situation
- To improve cross-line display caused by open circuit of LED
- Simplify the PCB wiring complexity of LED module
- Package type: SOP16
- ESD ≥ 8KV

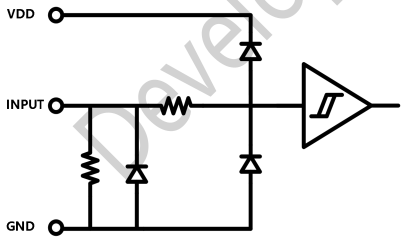
3 Applications

- High refresh rate LED display
- Full-color LED Displays
- For high density and small pitch LED module display

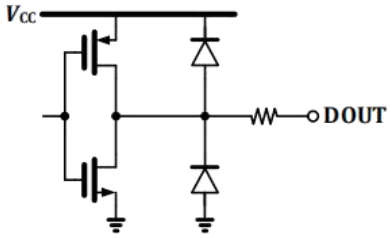
4 Circuit schematic diagram

4.1 Input and Output Equivalent Circuit

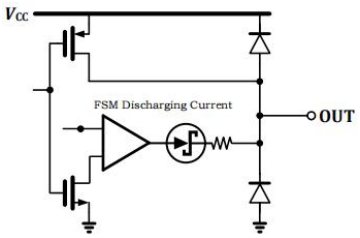
DIN,DCK,RCK terminals



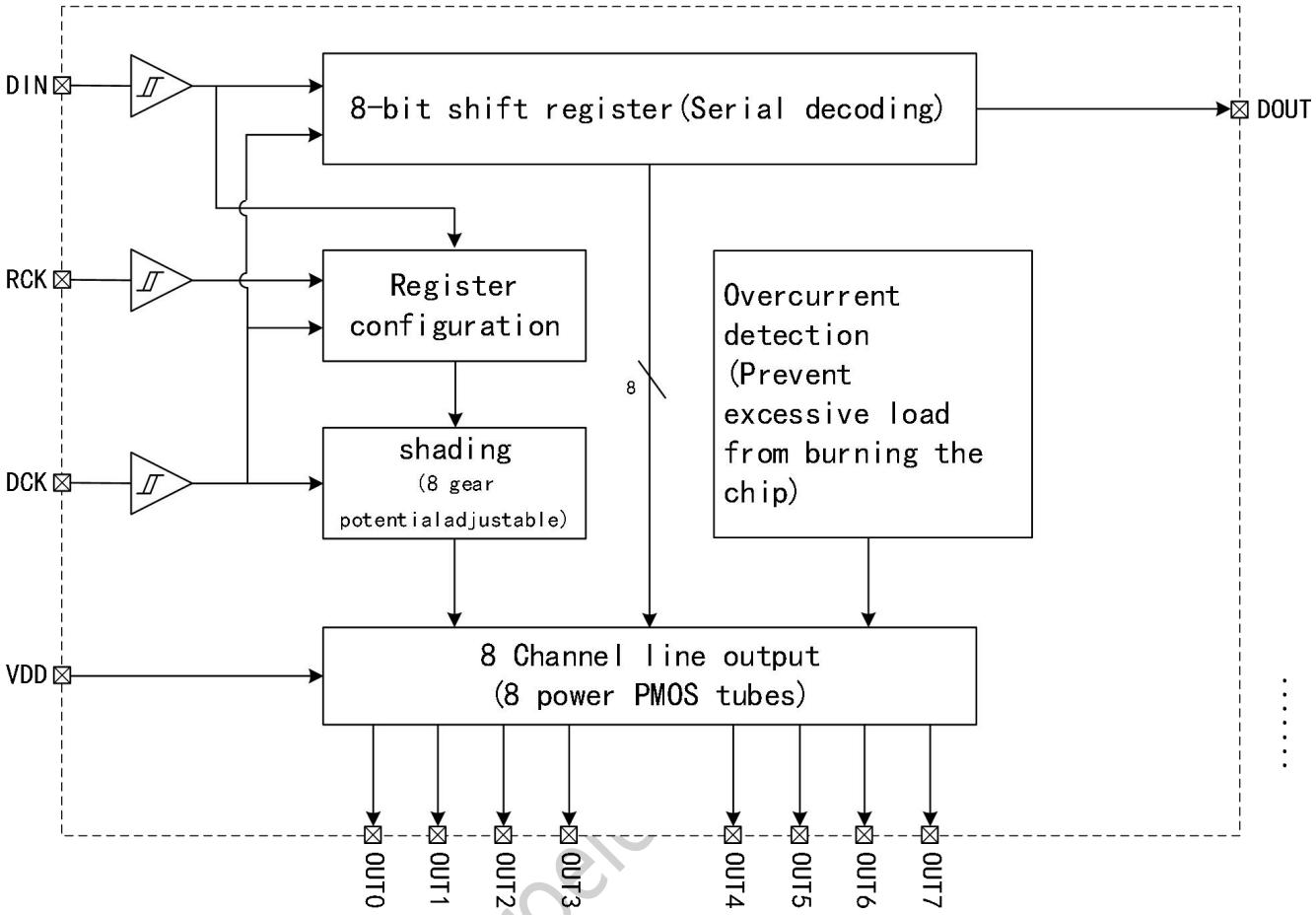
DOUT output terminal



OUT0~7 output terminal



4.2 Internal Circuit Block Diagram



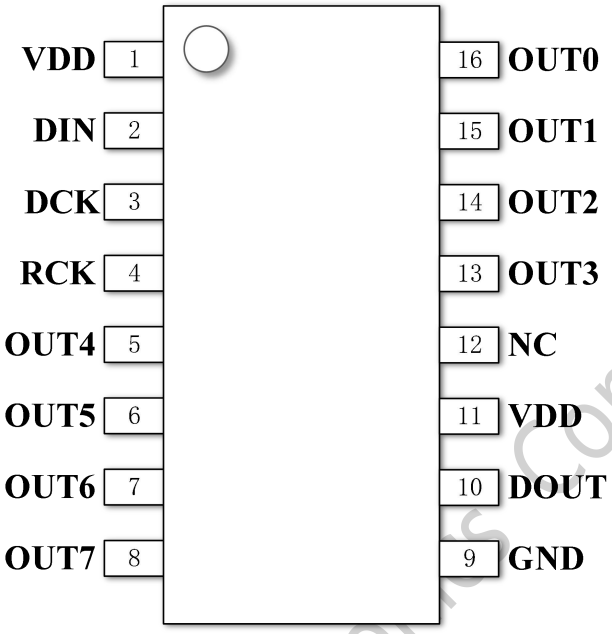
Contents

Revision History

Edition	Revised date	Reviser	Revised Contents
V1.0	2024.09	WM	1.Initial Version
V1.1	2024.09	WM	1.Modify the DC Electrical Characteristics
V1.2	2024.12	WM	1.Modify the packaging
V1.3	2025.04	WM	1.Modify the Working voltage 2.Updata of packaging size
V1.4	2025.06	WM	1.Modify the overview

5 Product Description

• Pin configuration



SOP16

• Description of pin functions

SOP16 Pin no	Pin name	Pin description
1，11	VDD	Power input
2	DIN	Data input
3	DCK	Serial signal clock input
4	RCK	Blanking register equipped with clock input
5~8，13~16	OUT0~OUT7	Output
9	GND	Earth
10	DOUT	Serial Data Output
12	NC	Empty pin

• Package Information

Product name	Packaging mode	Packaging method	Quantity/tray	Moisture sensitivity grade
DP32021	SOP16	Tape	4000	MSL=3

- **Product marking**

SOP16

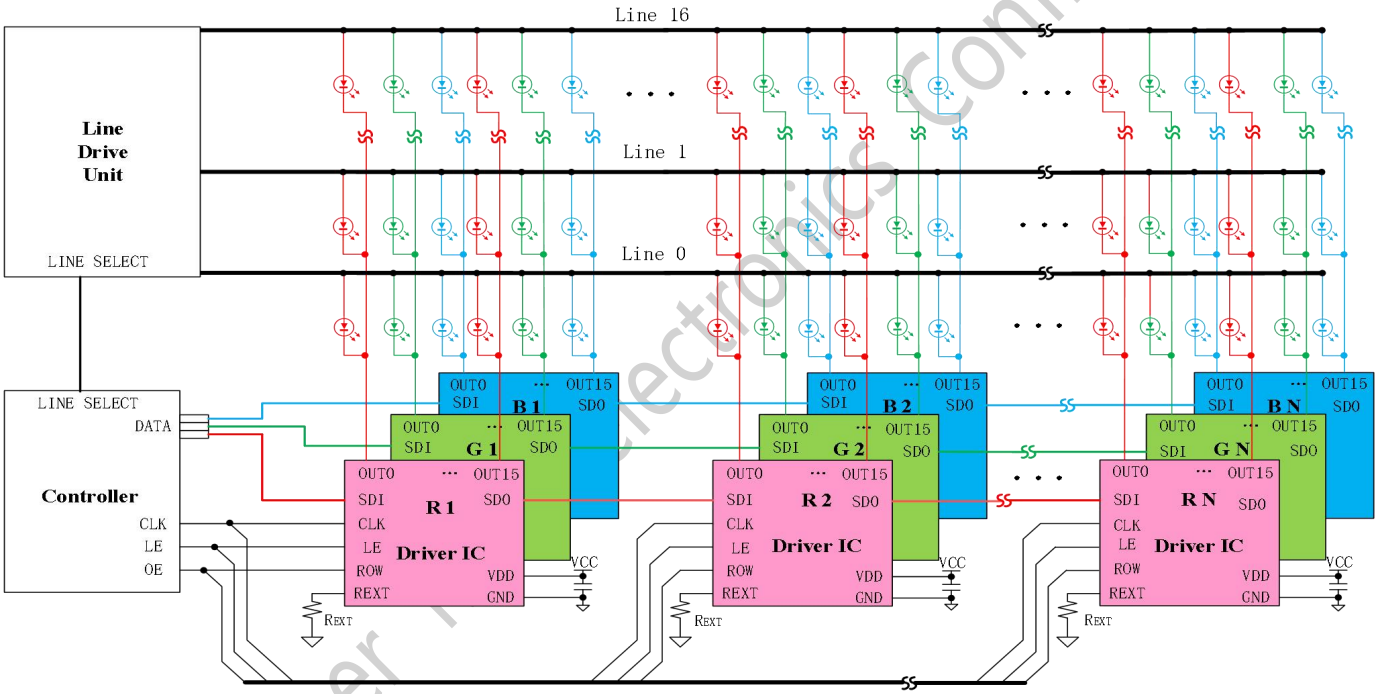
DP32021 is the product name

XXXXXX represents the product batch number

6 Proposed Application Circuit

LED scanning screen is widely used indoors to reduce costs; however, parasitic capacitance of LED anode usually produces an instantaneous discharge path when scanning, causing display trailing smear; users can use DP32021 with discharge circuit function and refer to the recommended application circuit of scanning screen in below figure in combination with the drive chip DP3365S of constant current with pre-charging function, so that the trailing smear can be eliminated from bottom to top completely.

DP32021 is an integrated power chip with 8-channel output. To avoid excessive heat accumulation, it is recommended to use a display screen with 16-scan or above and pay attention to the temperature during use.



LED application block diagram with 16-scan

7 Parameter List

7.1 Maximum Limit Parameter

Project	Symbols	Standard value	Unit
Power supply voltage	V_{CC}	0~6.0	V
Input Voltage	V_{IN}	-0.4~V_{DD}+0.4	V
Continuous working output current	I_D	-4	A
Instantaneous maximum output current	I_{OUT_MAX}	-4.5	A
Power Loss	PD	<600	mW
Package thermal resistance	$R_{th(j-a)}$	80	℃/W
Operating temperature	T_{opr}	-40~85	℃
Storage Temperature	T_{stg}	-40~150	℃
Human body model (HBM)	V_{ESD}	≥8	KV

1. All the voltage value setting based on Chip ground port (GND) as reference, the test temperature of the maximum limit parameter is 25℃;
2. Application exceed the above specified value, may cause permanent damage to components, extending the operating life under absolute maximum conditions may reduce the reliability of the components. These are only part of the specified values, and do not support the functional operation of other conditions beyond the specification.
3. SMD components, soldering peak temperature must be lower than 260℃, temperature curve as standard J-STD-020, and factory decides by itself, take the reference by actual situation and solder paste manufacture' s suggestion.

7.2 Recommended Work Scope

Project	Symbols	Conditions	Min value	Standard value	Max value	Unit
Power supply voltage	V_{CC}	—	2.8	5.0	5.5	V
Output terminal voltage (DOUT)	V_{DOUT}	—	0.7	—	V_{DD}	V
Output terminal current (DOUT)	I_{OH}	V_{OH} =V_{DD} -0.5V	—	-16	—	mA
	I_{OL}	V_{OL} =0.5V	—	20	—	
Input voltage (DIN,DCK,RCK)	V_{IH}	V_{DD}=2.8V~5.5V	0.7 V_{DD}	—	V_{DD}	V
	V_{IL}		0	—	0.3V_{DD}	

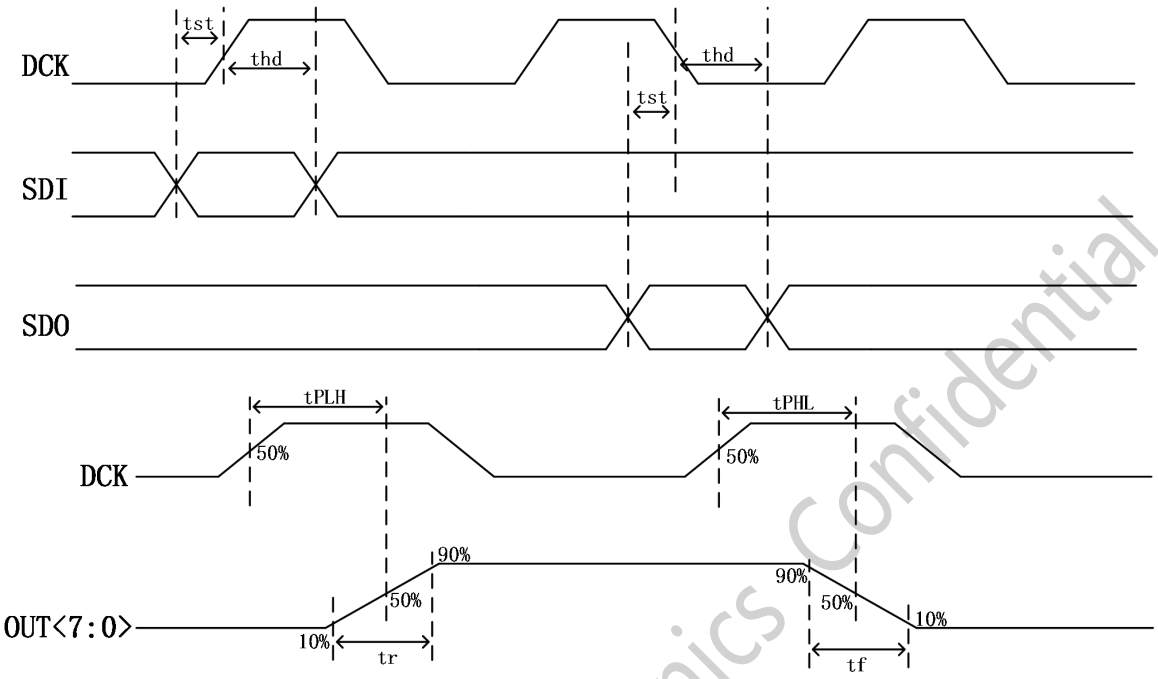
7.3 DC Electrical Characteristics (VDD=5.0V)

Project		Symbols	Conditions	Min value	Standard value	Max value	Unit
Logic power supply voltage		V_{DD}	—	2.8	5.0	5.5	V
Power terminal current		I_{DD_OFF}	All output are set low	—	400	—	uA
Gate opening voltage		$V_{GS(th)}$	V_{DS}=VGS,I_D=250uA	—	-0.7	-0.9	V
Source-drain pole conduction resistance		$R_{DS(on)[1:7]}$	V_{GS}=-5.0V, I_{OUT}=-1.0A	—	73	76	mΩ
Input voltage	High level	V_{IH}	Logic potential	0.7 V_{DD}	—	V_{DD}	V
	Low level	V_{IL}		0	—	0.3 V_{DD}	

7.4 Dynamic Property (Without special instructions, VDD=3.5V~5V, Ta=25℃)

Project	Symbols	Test conditions	Min value	Standard value	Max value	Unit
Output rise delay	t_{PLH}	VDD=5.0V CL=12pF	-	50	-	ns
Output drop delay	t_{pHL}		-	100	-	ns
Output rising edge	t_r		-	60	-	ns
Output drop edge	t_f		-	400	-	ns
Setup time	t_{st}		30	-	-	ns
Hold time	t_{hd}		30	-	-	ns

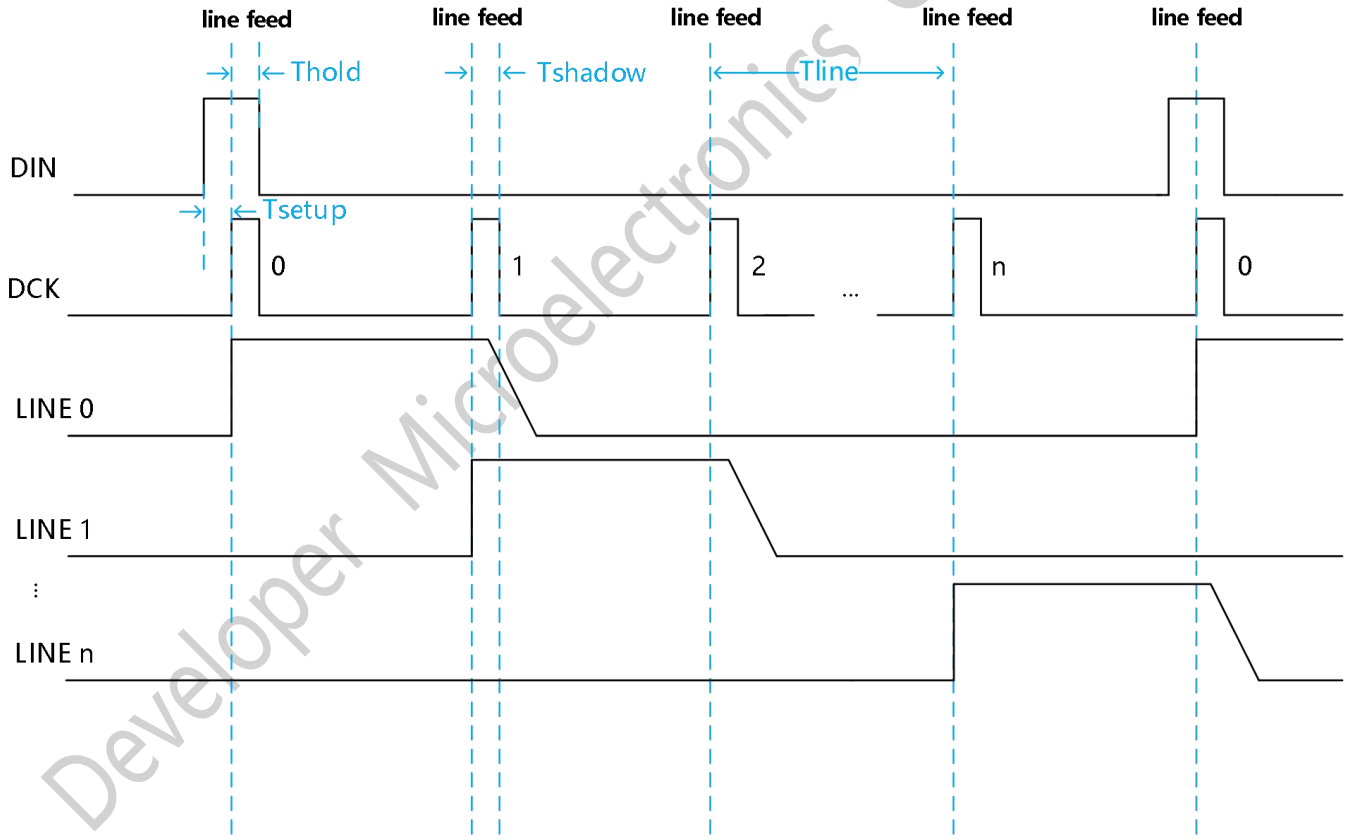
8 Time Series Pattern



9 Line Feed Control and Fade Time

DP32021 is a row pipe drive of serial decoding of common anode display screen; each line feed is fixed as sending one DCK, with high channel output efficiency; input data DIN to output data DOUT is fixed as rising edge interval of 8 DCK.

Symbols	Description	Min value	Max value
Tshadow	Ghosting reduction time is equal to DCK high level width	500ns	-
Tsetup	Setup time	60ns	-
Thold	Hold time	60ns	-

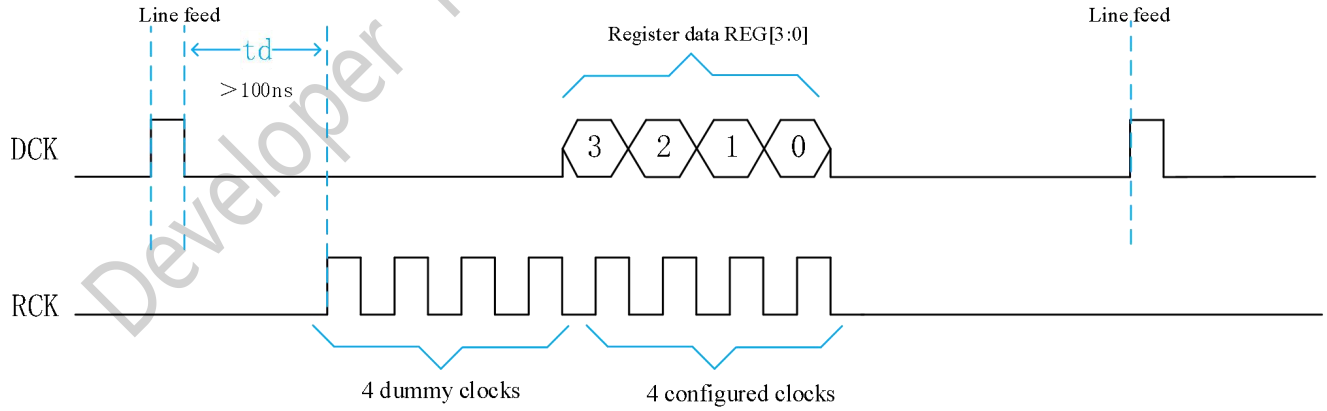


10 Register Configuration

DP32021 equipped with 4bit register:

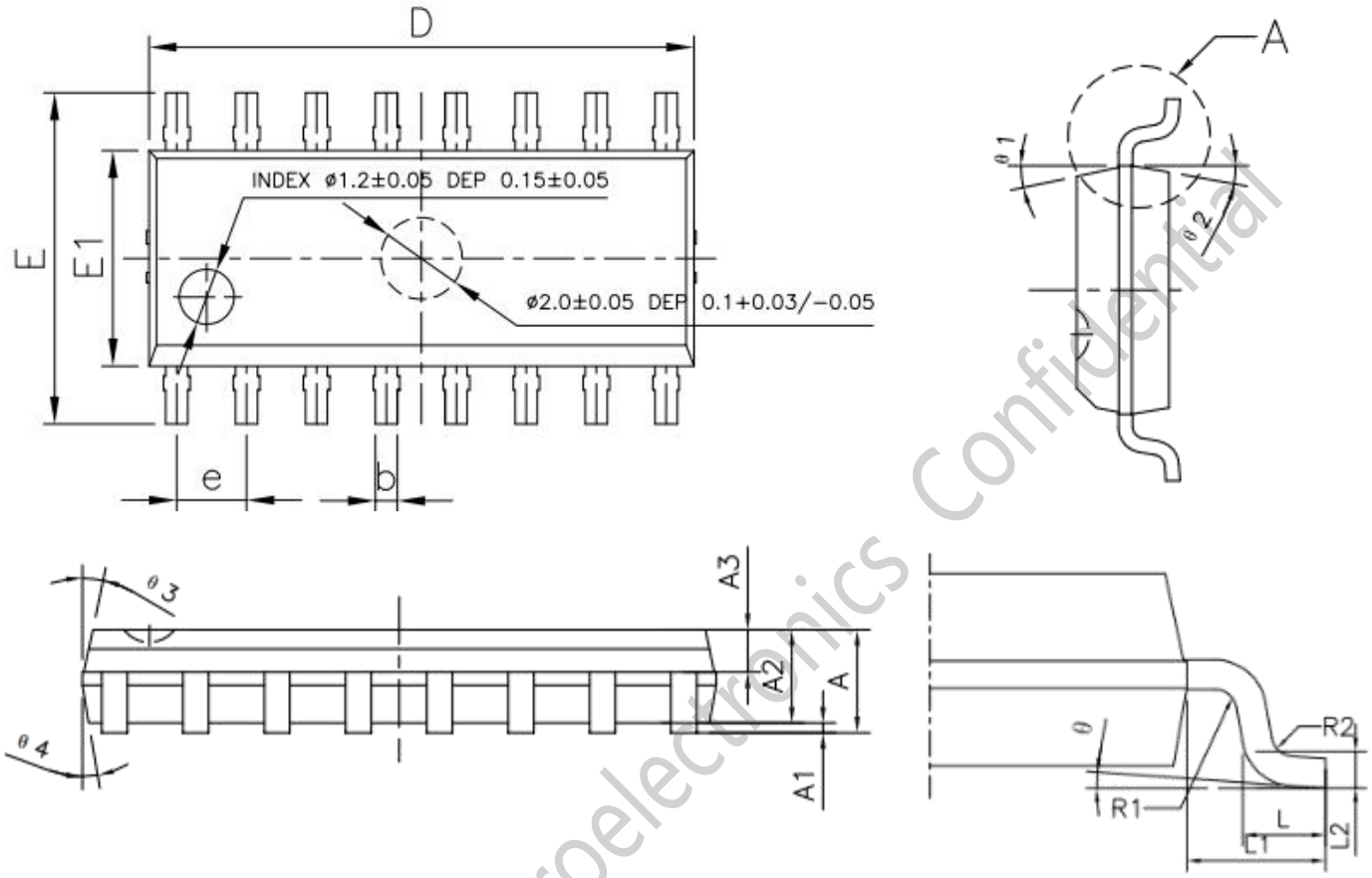
BIT	Name	Default	Description		
3	VR_UP [2]	1’ b1	Circuit of pull-up ghosting reduction refers to the highest bit in potential configuration register VR_ UP[2:0]		
2	reserved	1’ b0	reserved		
1:0	VR_UP [1:0]	2’ b10	Reference potential of pull-up ghosting reduction circuit can be configured as (Vdd=5V) according to register VR_ UP [2:0]		
			0000：Vdd*7/20 =1.75V 0001：Vdd*8/20 =2.0V 0010：Vdd*9/20 =2.25V 0011：Vdd*10/20 =2.5V	1000：Vdd*11/20 =2.75V 1001：Vdd*12/20 =3.0V 1010：Vdd*13/20 =3.25V 1011：Vdd*15/20 =3.5V	Default 2.75V **Data pin correspondence** SDI corresponds to C signal of 3-8 decoding DCK corresponds to A signal of 3-8 decoding RCK corresponds to B signal of 3-8 decoding

The mode of configuration register: When DCK is low, 8 clocks sent to RCK (4 dummy clocks+4 register configuration clocks) send register data via DCK during the 4 clocks period of register configuration.



11 Packaging Size

SOP16



Symbol	Min	Nom	Max
A	-	-	1.70
A1	0.10	0.15	0.20
A2	1.42	1.45	1.48
A3	0.62	0.65	0.68
b	0.38	-	0.51
D	9.85	9.90	9.95
E	5.90	6.00	6.10
E1	3.87	3.90	3.93
e	1.24	1.27	1.30
L	0.50	0.60	0.70
L1	1.05REF		
L2	0.25REF		
Θ	0°	-	8°
Θ1-Θ4	12°REF		
R1	0.15REF		
R2	0.15REF		

12 Official Announcement

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