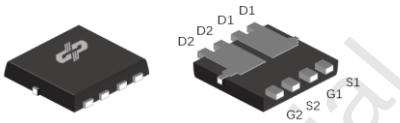
DP4904MTLD

40V Dual P + N-channel MOSFET

Product Summary

Part #	V_{DS}	$R_{DS(on).typ}$ ($@V_{GS}$=10V)	$R_{DS(on).typ}$ ($@V_{GS}$=4.5V)	I_D
DP4904MTLD	40V	16mΩ	22mΩ	20A
	-40V	32mΩ	39mΩ	-15A

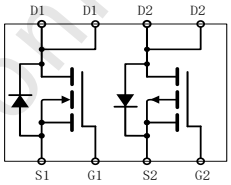
PDFN 3.3x3.3



Features

- Uses advanced MOSFET-DPMOS1 technology
- Extremely low $R_{DS(on)}$/High Speed Power Switching
- Excellent Q_gx$R_{DS(on)}$ product(FOM)
- Qualified according to JEDEC criteria

Schematic diagram



Applications

- PWM Applications
- Load Switch
- Power Management

Package Marking and Ordering Information

Part #	Marking	Package	Packing
DP4904MTLD	4904MTLD	PDFN 3.3x3.3	Reel/Tape

Halogen-Free

Absolute Maximum Ratings

Parameter	Symbol	NMOS	PMOS	Unit
Drain-source voltage	V_{DS}	40	-40	V
Continuous drain current				
T_C = 25°C	I_D	16	-15	A
T_C = 100°C		10	-9	
Pulsed drain current (T_C = 25°C, t_p limited by T_{jmax})	$I_{D\ pulse}$	64	60	A
Gate-Source voltage	V_{GS}	±20	±20	V
Power dissipation (T_C = 25°C)	P_{tot}	25	21	W
Operating junction and storage temperature	T_j , T_{stg}	-55...+150	-55...+150	°C

[1].EAS is tested at starting T_j = 25℃, V_{GS} = 10V.

Thermal Resistance

Parameter	Symbol	NMOS	PMOS	Unit
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	50	65	°C/W

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

NMOS

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	40	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{GS(th)}$	1	-	2.5	V	V_{DS}=V_{GS},I_D=250uA
Zero gate voltage drain current	I_{DSS}	- -	- -	1 100	μA	V_{DS}=40V,V_{GS}=0V T_j=25°C T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	±100	nA	V_{GS}=±20V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	16 22	21 30	mΩ	T_j=25°C V_{GS}=10V, I_D=6A V_{GS}=4.5V, I_D=6A
Gate resistance	R_g	-	5.5	-	Ω	V_{GS}=0V, V_{DS}=0V, f=1MHz
Dynamic Characteristic[2]						
Input Capacitance	C_{iss}	-	528	-	pF	VGS=0V, VDS=20V, f=1MHz
Output Capacitance	C_{oss}	-	102	-		
Reverse Transfer Capacitance	C_{rss}	-	21	-		
Gate Total Charge	Q_g	-	9	-	nC	VGS=10V, VDS=20V, ID=5A, f=1MHz
Gate-Source charge	Q_{gs}	-	1.3	-		
Gate-Drain charge	Q_{gd}	-	1.1	-		
Turn-on delay time	$t_{d(on)}$	-	3	-	ns	VGS=10V, VDD=20V, RG_ext=2.7Ω
Rise time	t_r	-	2	-		
Turn-off delay time	$t_{d(off)}$	-	16	-		
Fall time	t_f	-	7	-		

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.8	1.2	V	V_{GS}=0V,I_{SD}=5A

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

PMOS

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	-40	-	-	V	V_{GS}=0V, I_D=-250uA
Gate threshold voltage	$V_{GS(th)}$	-1	-	-2.5	V	V_{DS}=V_{GS},I_D=-250uA
Zero gate voltage drain current	I_{DSS}	- -	- -	-1 -100	μA	V_{DS}=-40V,V_{GS}=0V T_j=25°C T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	±100	nA	V_{GS}=±20V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	32 39	43 53	mΩ	T_j=25°C V_{GS}=-10V, I_D=-6A V_{GS}=-4.5V, I_D=-5A
Gate resistance	R_g	-	8	-	Ω	V_{GS}=0V, V_{DS}=0V, f=1MHz
Dynamic Characteristic[2]						
Input Capacitance	C_{iss}	-	1113	-	pF	VGS=0V, VDS=-20V, f=1MHz
Output Capacitance	C_{oss}	-	442	-		
Reverse Transfer Capacitance	C_{rss}	-	43	-		
Gate Total Charge	Q_g	-	14	-	nC	VGS=-10V, VDS=-20V, ID=-5A, f=1MHz
Gate-Source charge	Q_{gs}	-	1.8	-		
Gate-Drain charge	Q_{gd}	-	1.9	-		
Turn-on delay time	$t_{d(on)}$	-	8	-	ns	VGS=-10V, VDD=-20V, RG_ext=2.7Ω
Rise time	t_r	-	13	-		
Turn-off delay time	$t_{d(off)}$	-	16	-		
Fall time	t_f	-	6	-		

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	-	-1.2	V	V_{GS}=0V,I_{SD}=-5A

Typical Performance Characteristics

NMOS

Fig 1: Output Characteristics

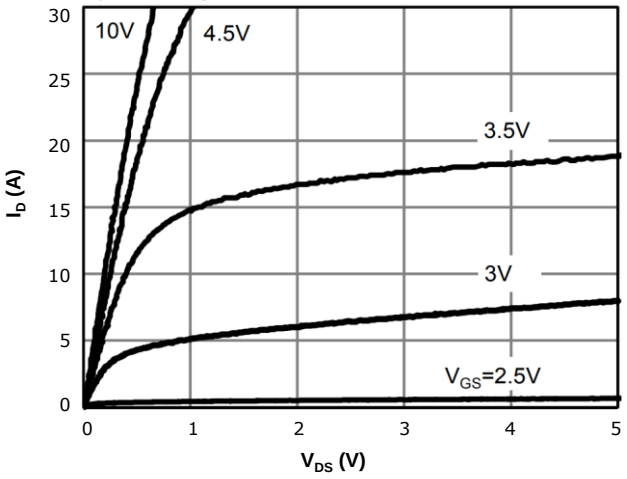


Fig 2: Transfer Characteristics

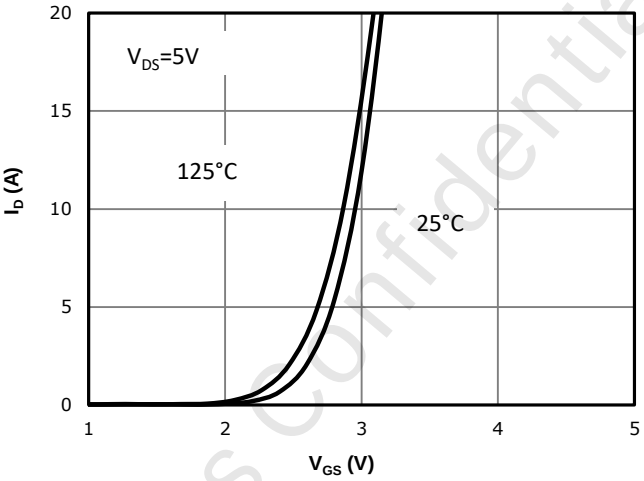


Fig 3: Rds(on) vs Drain Current and Gate Voltage

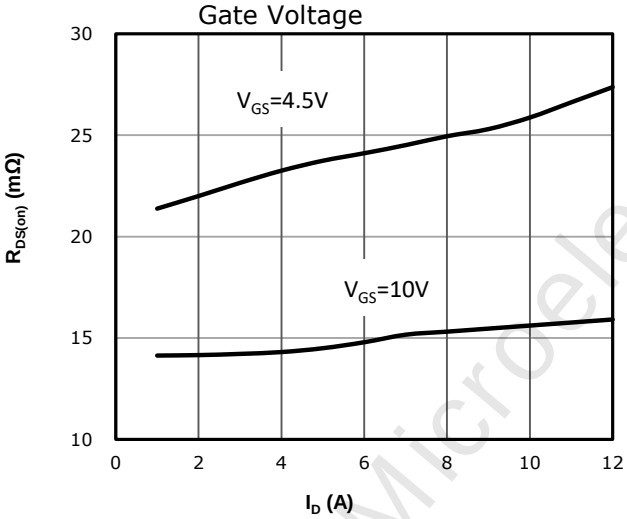


Fig 4: Rds(on) vs Gate Voltage

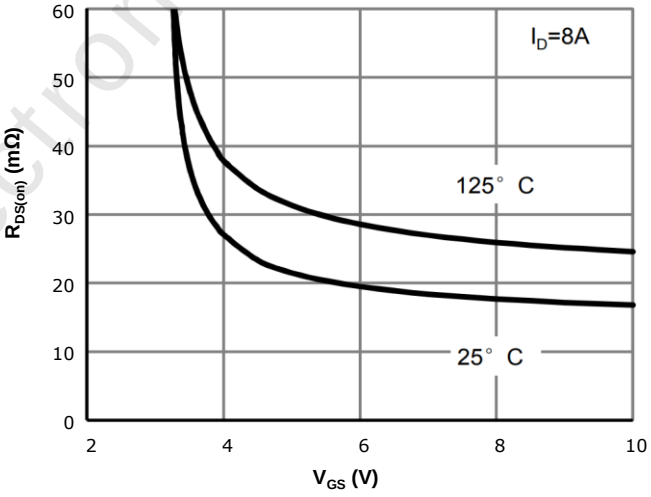


Fig 5: Rds(on) vs. Temperature

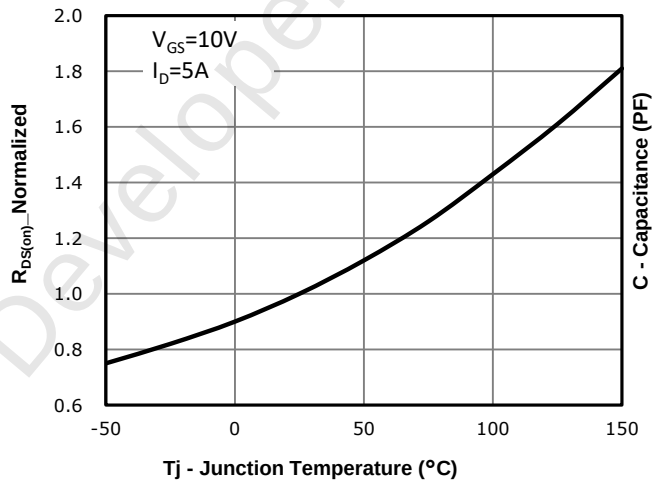
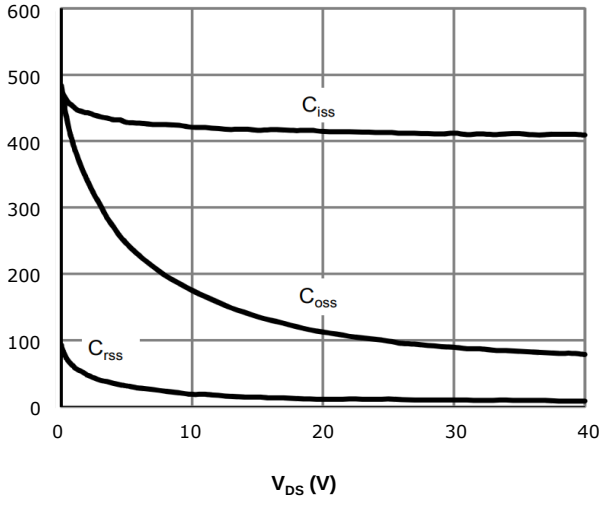


Fig 6: Capacitance Characteristics



PMOS

Fig 1: Output Characteristics

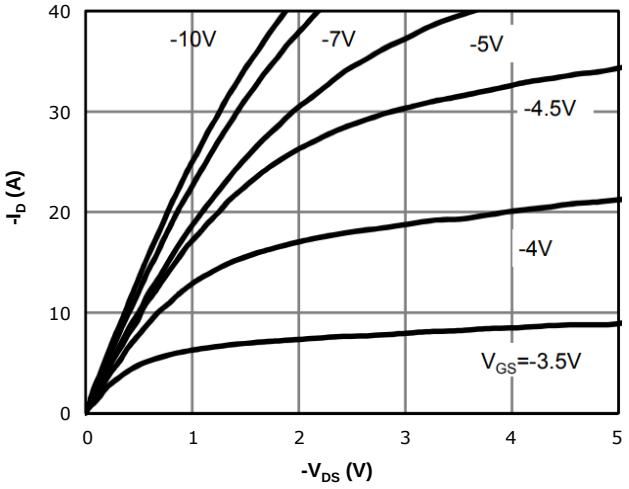


Fig 2: Transfer Characteristics

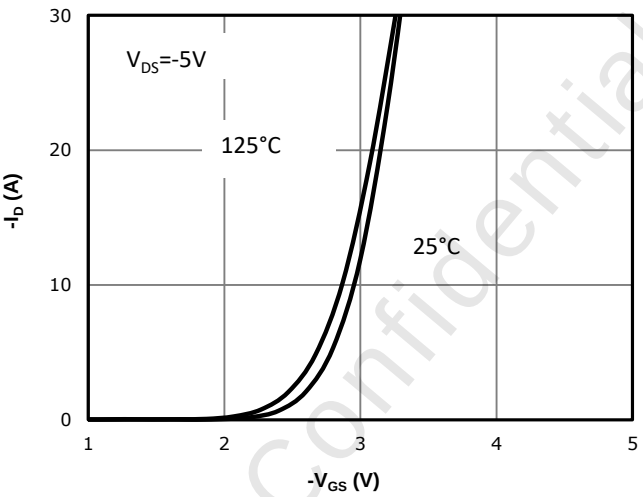


Fig 3: Rds(on) vs Drain Current and Gate Voltage

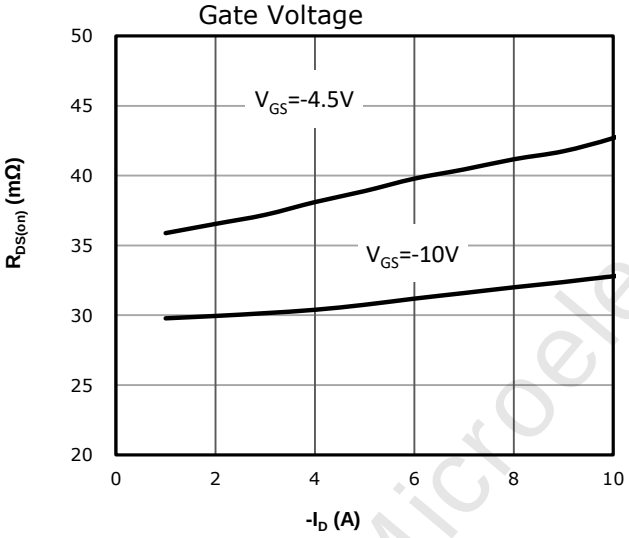


Fig 4: Rds(on) vs Gate Voltage

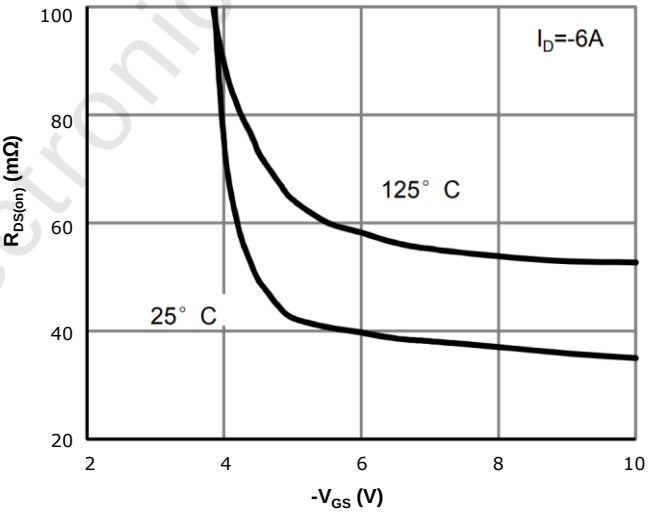


Fig 5: Rds(on) vs. Temperature

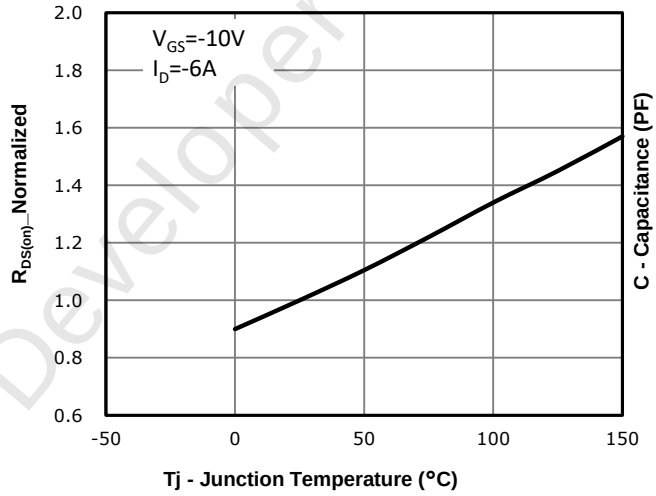
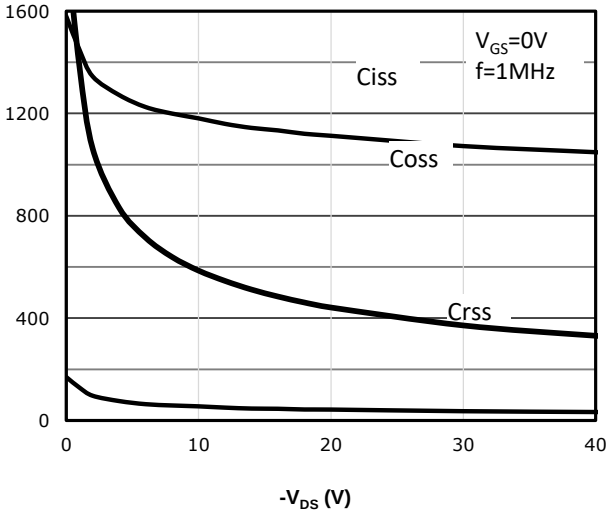
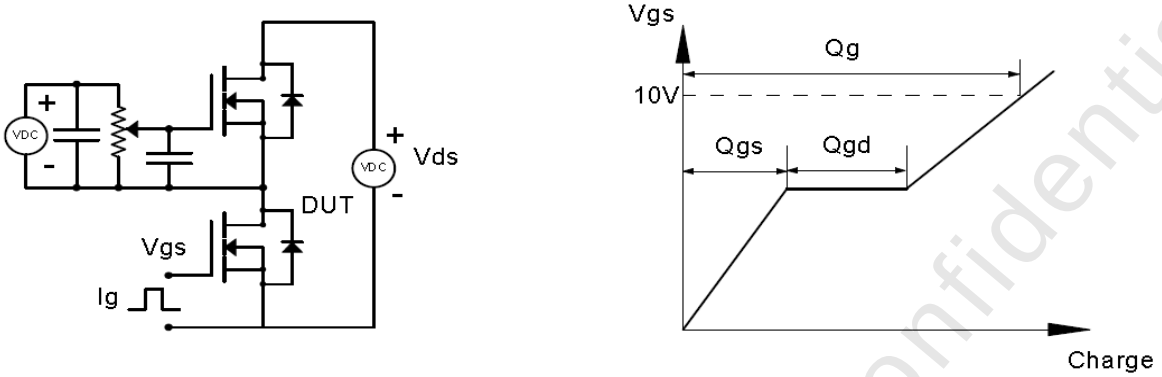


Fig 6: Capacitance Characteristics

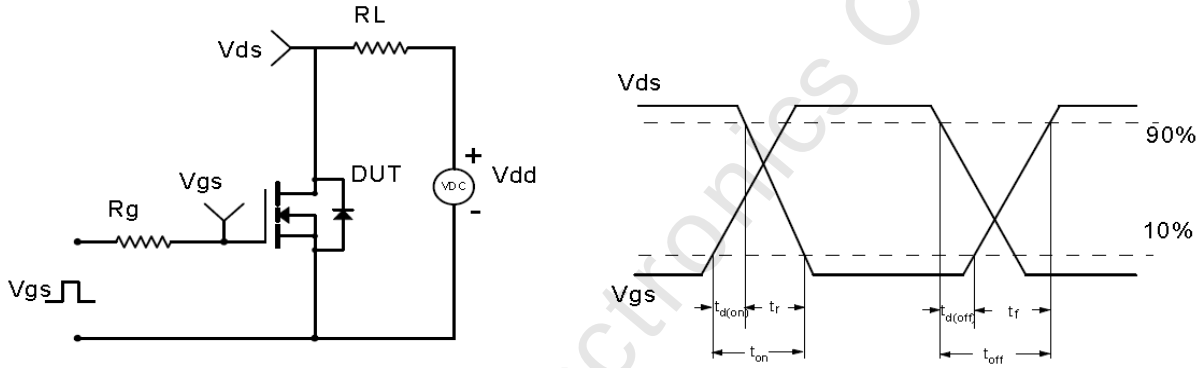


Test Circuit & Waveform

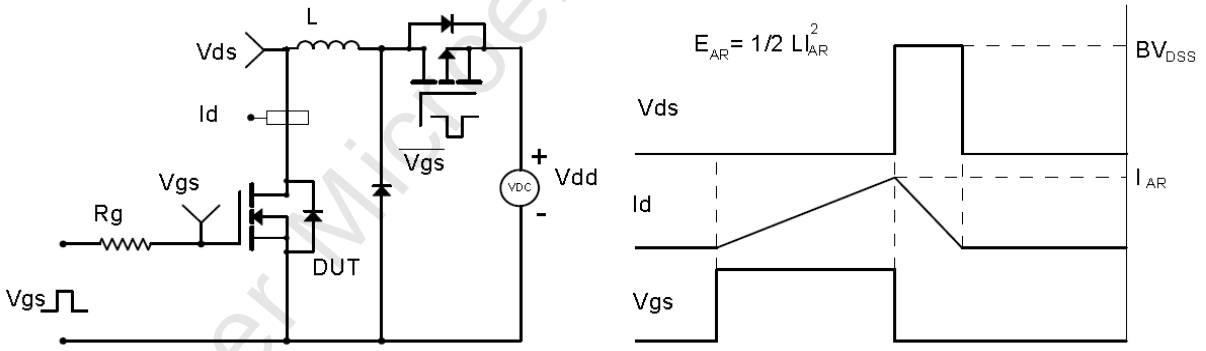
Gate Charge Test Circuit & Waveform



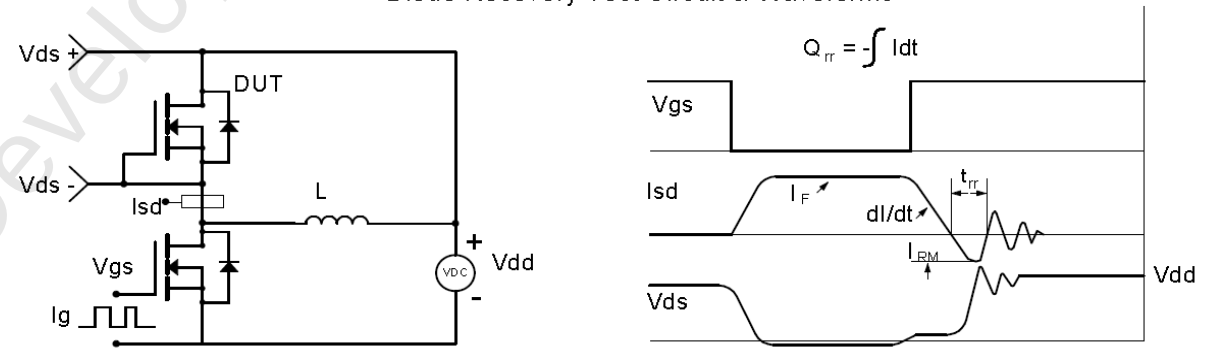
Resistive Switching Test Circuit & Waveforms



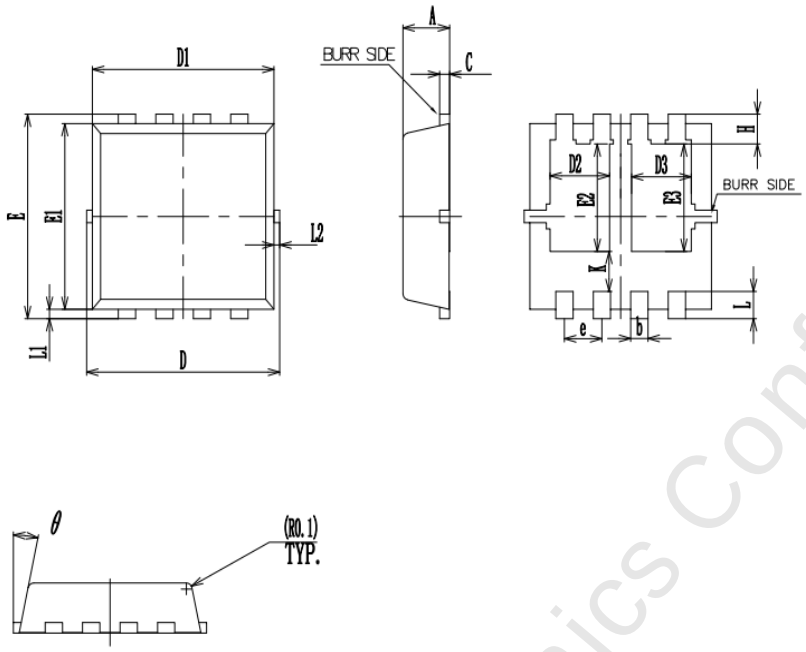
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

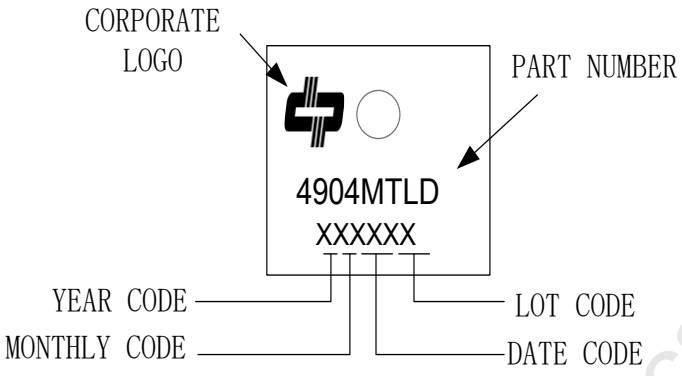


Package Outline: PDFN 3.3x3.3



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.70	0.90	0.028	0.035
b	0.25	0.35	0.010	0.014
c	0.14	0.20	0.006	0.008
D	3.15	3.45	0.124	0.136
D1	3.05	3.25	0.120	0.128
D2	0.94	1.14	0.037	0.045
D3	0.94	1.14	0.037	0.045
e	0.65 BSC.		-	
E	3.20	3.40	0.126	0.134
E1	2.90	3.10	0.114	0.122
E2	1.64	1.84	0.065	0.072
E3	1.64	1.84	0.065	0.072
H	0.38	0.58	0.015	0.023
K	0.59	0.79	0.023	0.031
L	0.25	0.55	0.010	0.022
L1	0.10	0.20	0.004	0.008
L2	-	0.15	-	0.006
θ	8°	12°	8°	12°

Part Marking Information



Revision History

Revison	Major changes
1.0	Release for formal version

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