

**Product Summary**

Part #	V <sub>DS</sub>	R <sub>DS(on).typ</sub> (@V <sub>GS</sub> =10V)	R <sub>DS(on).typ</sub> (@V <sub>GS</sub> =4.5V)	I <sub>D</sub>
DP055N04FTL	40V	4.8mΩ	6mΩ	70A

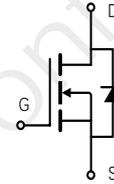
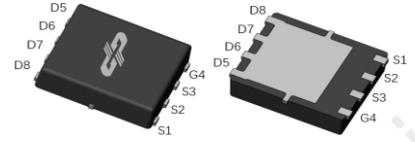
**Features**

- Uses advanced trench MOSFET technology
- Extremely low on-resistance R<sub>DS(on)</sub>
- Excellent Q<sub>g</sub>xR<sub>DS(on)</sub> product(FOM)
- Qualified according to JEDEC criteria

**Applications**

- Motor control and drive
- Battery management
- UPS (Uninterruptible Power Supplies)

DFN 5x6



100% Avalanche Tested

 100% R<sub>g</sub> Tested

**Package Marking and Ordering Information**

Part #	Marking	Package	Packing
DP055N04FTL	055N04FTL	DFN 5x6	Tape&Reel


**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Drain-source voltage	V <sub>DS</sub>	40	V
Continuous drain current	I <sub>D</sub>	70	A
T <sub>C</sub> = 25°C		45	
T <sub>C</sub> = 100°C			
Pulsed drain current (T <sub>C</sub> = 25°C, t <sub>p</sub> limited by T <sub>jmax</sub> )	I <sub>D pulse</sub>	280	A
Avalanche energy, single pulse (L=0.5mH, R <sub>g</sub> =25Ω) <sup>[1]</sup>	E <sub>AS</sub>	81	mJ
Gate-Source voltage	V <sub>GS</sub>	±20	V
Power dissipation (T <sub>C</sub> = 25°C)	P <sub>tot</sub>	58	W
Operating junction and storage temperature	T <sub>j</sub> , T <sub>stg</sub>	-55...+150	°C

[1].EAS is tested at starting T<sub>j</sub> = 25°C, V<sub>GS</sub> = 10V.

**Thermal Resistance**

Parameter	Symbol	Max	Unit
Thermal resistance, Junction-to-Case.	$R_{thJC}$	2.2	°C/W
Thermal resistance, junction – ambient(min. footprint)	$R_{thJA}$	48	

**Electrical Characteristic (at  $T_j = 25\text{ }^\circ\text{C}$ , unless otherwise specified)**

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

**Static Characteristic**

Drain-source breakdown voltage	$BV_{DSS}$	40	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=40V, V_{GS}=0V$ $T_j=25^\circ C$ $T_j=150^\circ C$
Gate-source leakage current	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	4.8	5.7	mΩ	$V_{GS}=10V, I_D=30A$ $V_{GS}=4.5V, I_D=25A$
Gate resistance	$R_g$	-	1.1	3	Ω	$V_{GS}=0V, V_{DS}=0V,$ $f=1MHz$
Transconductance <sup>[2]</sup>	$g_{fs}$	-	37	-	S	$V_{DS}=5V, I_D=20A$

**Dynamic Characteristic<sup>[2]</sup>**

Input Capacitance	$C_{iss}$	-	2233	-	pF	$V_{GS}=0V, V_{DS}=20V,$ $f=1MHz$
Output Capacitance	$C_{oss}$	-	169	-		
Reverse Transfer Capacitance	$C_{rss}$	-	154	-		
Gate Total Charge	$Q_g$	-	43	-	nC	$V_{GS}=10V, V_{DS}=20V,$ $I_D=18A, f=1MHz$
Gate-Source charge	$Q_{gs}$	-	7	-		
Gate-Drain charge	$Q_{gd}$	-	8	-		
Turn-on delay time	$t_{d(on)}$	-	7	-	ns	$V_{GS}=10V, V_{DD}=20V,$ $R_{G\_ext}=2.7\Omega$
Rise time	$t_r$	-	27	-		
Turn-off delay time	$t_{d(off)}$	-	58	-		
Fall time	$t_f$	-	22	-		

**Body Diode Characteristic**

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	$V_{SD}$	-	0.8	1.3	V	$V_{GS}=0V, I_{SD}=20A$
Diode continuous forward current	$I_S$	-	-	70	A	TC = 25°C
Diode pluse current	$I_{S\ pluse}$	-	-	280	A	TC = 25°C
Body Diode Reverse Recovery Time <sup>[2]</sup>	$t_{rr}$	-	19	-	ns	$I_F=20A, di/dt=100A/\mu s$
Body Diode Reverse Recovery Charge <sup>[2]</sup>	$Q_{rr}$	-	12	-	nC	

[2]. Defined by design. Not subject to production test

**Typical Performance Characteristics**

Fig 1: Output Characteristics

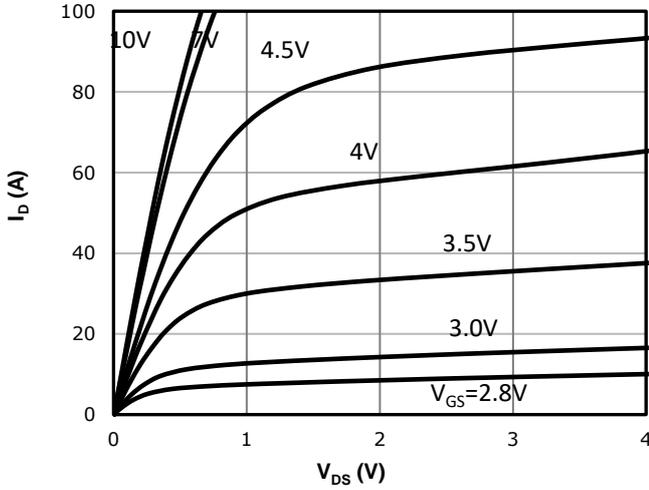


Fig 2: Transfer Characteristics

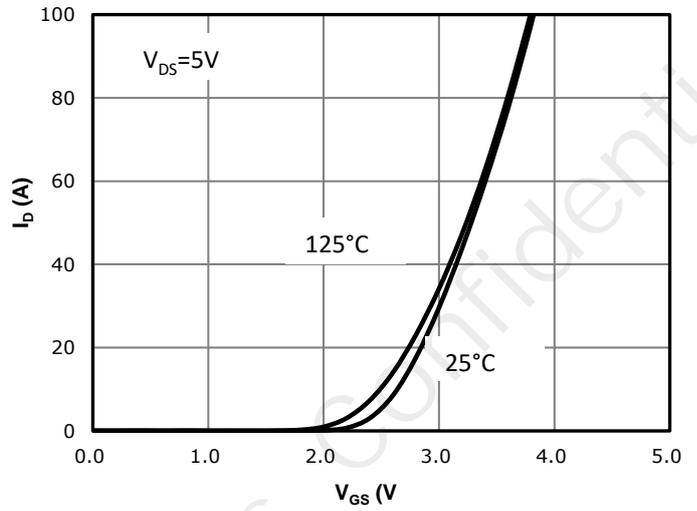


Fig 3: Rds(on) vs Drain Current and Gate Voltage

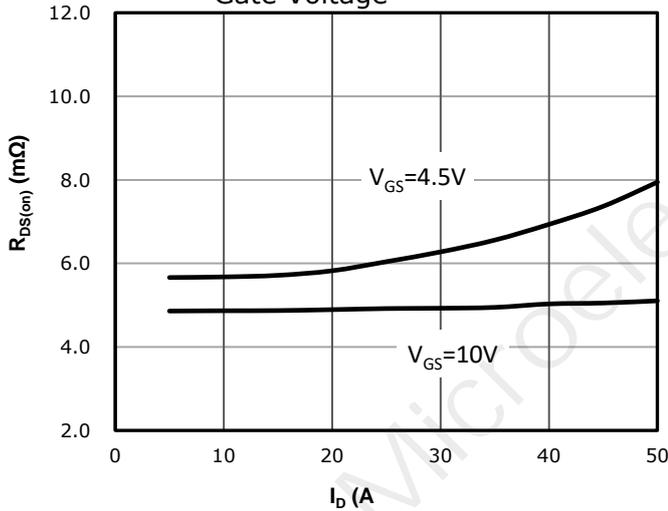


Fig 4: Rds(on) vs Gate Voltage

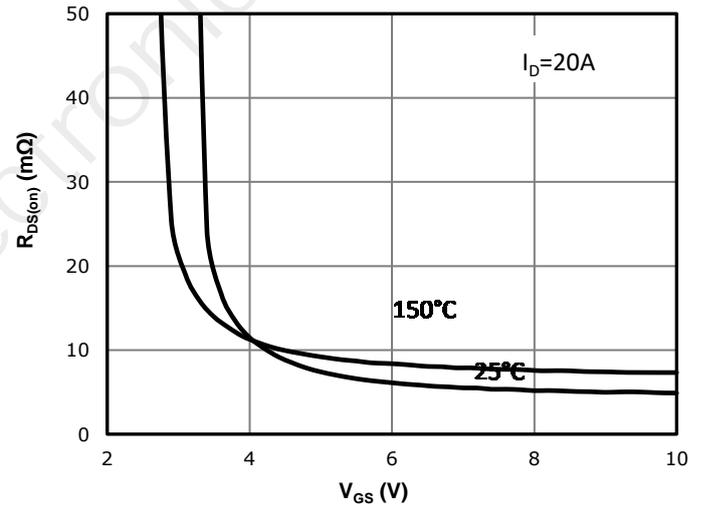


Fig 5: Rds(on) vs. Temperature

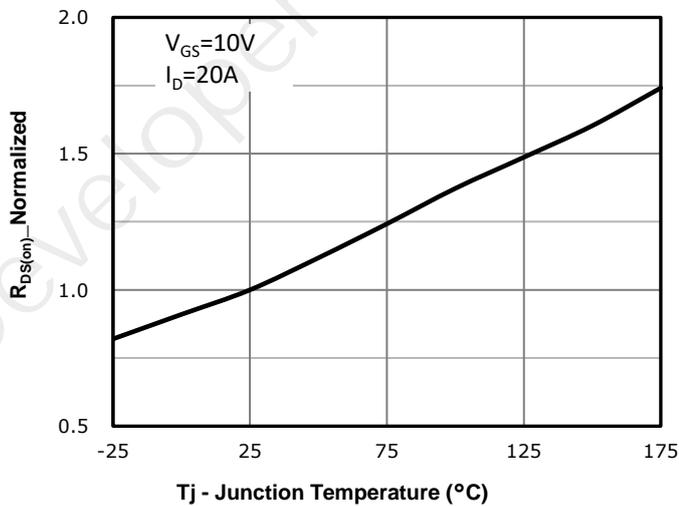


Fig 6: Capacitance Characteristics

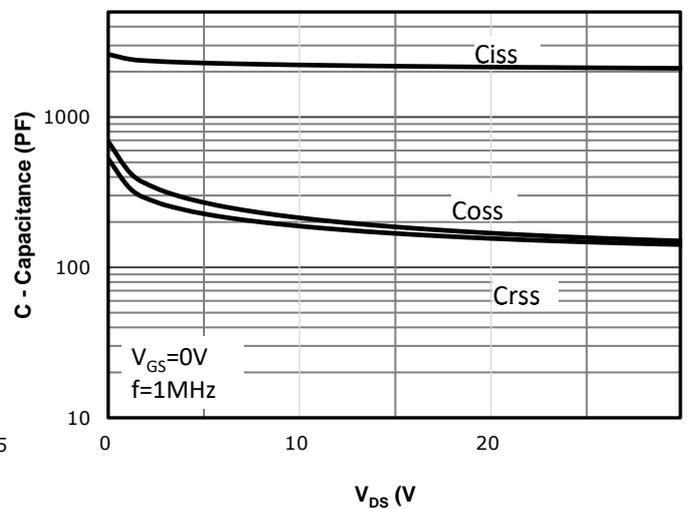


Fig 7: Gate Charge Characteristics

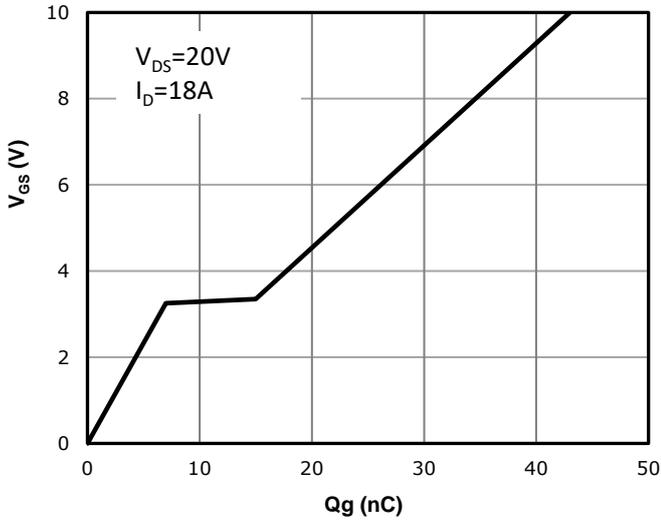


Fig 8: Body-diode Forward Characteristics

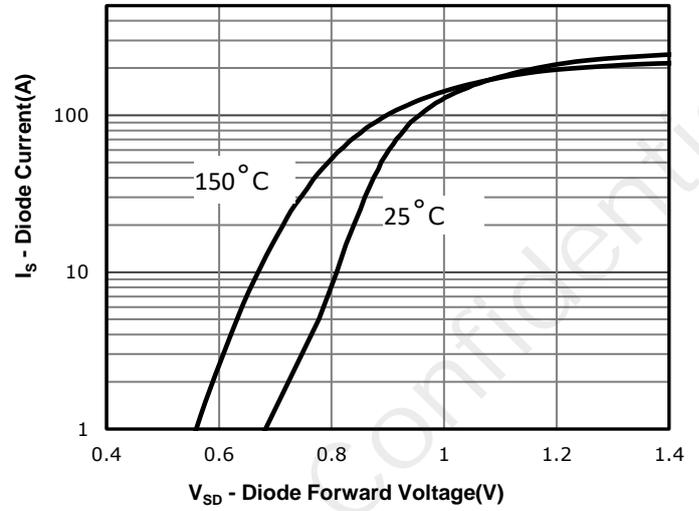


Fig 9: Power Dissipation

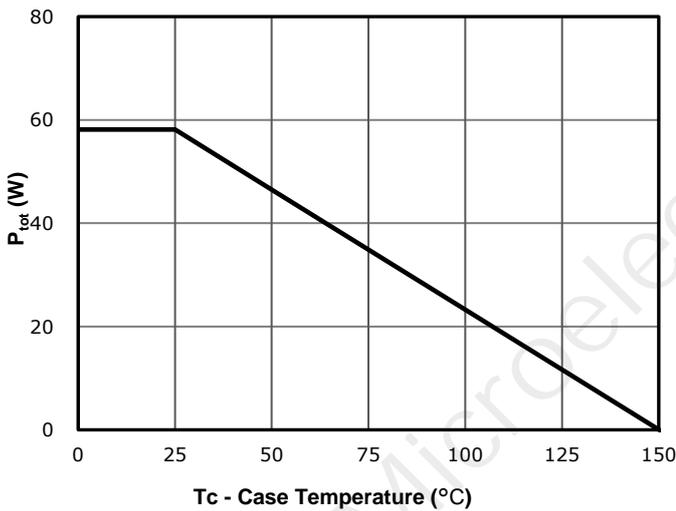


Fig 10: Drain Current Derating

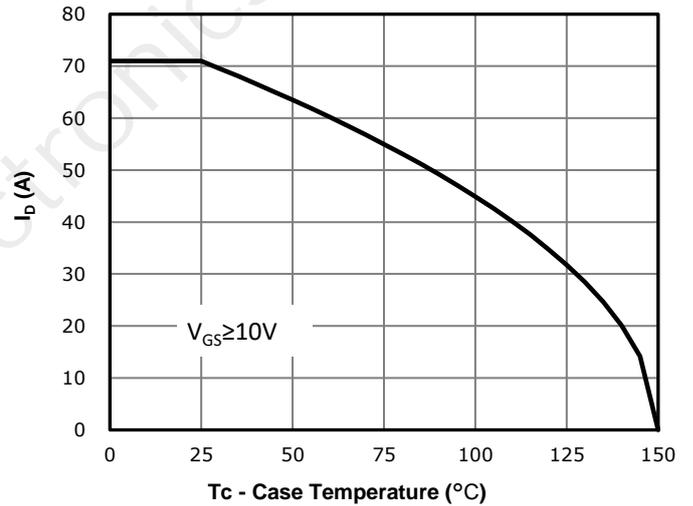


Fig 11: Safe Operating Area

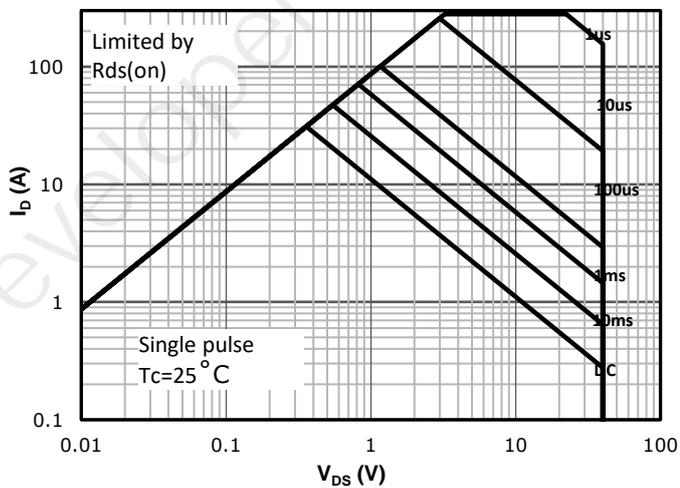
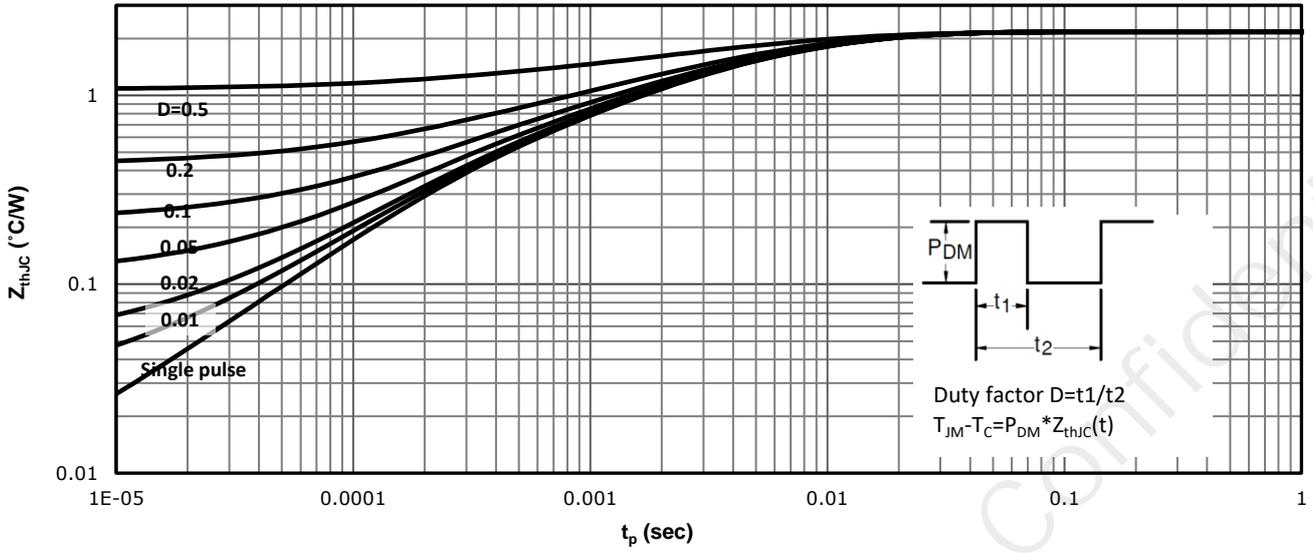
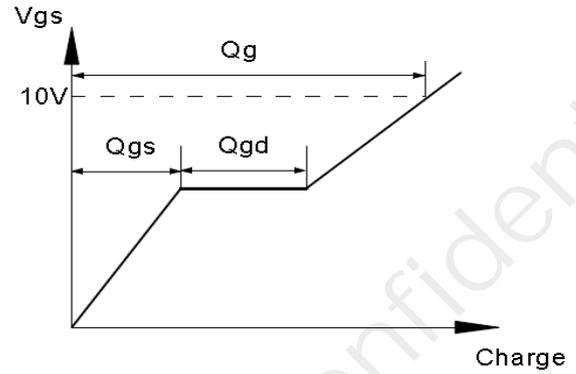
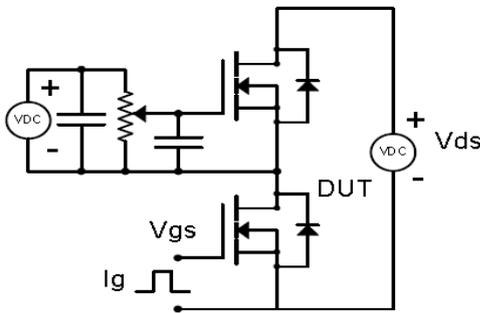


Fig 12: Max. Transient Thermal Impedance

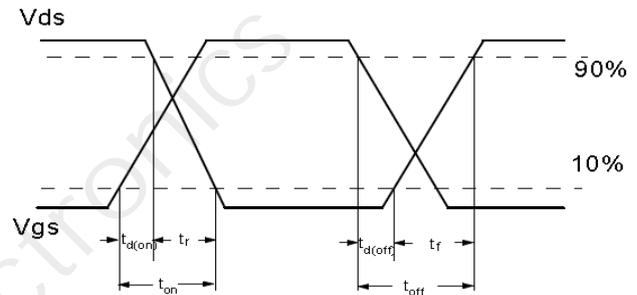
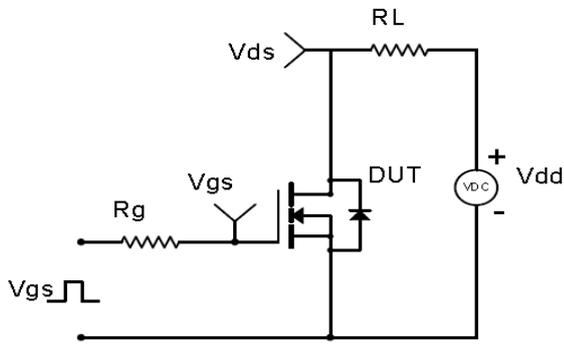


**Test Circuit & Waveform**

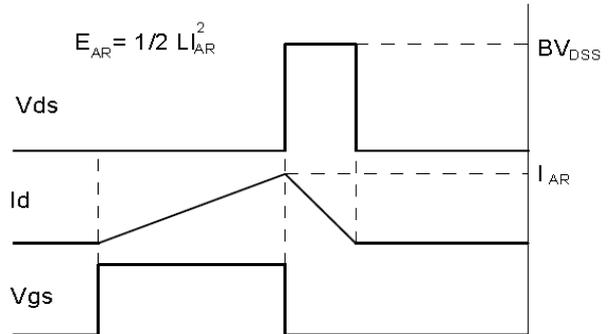
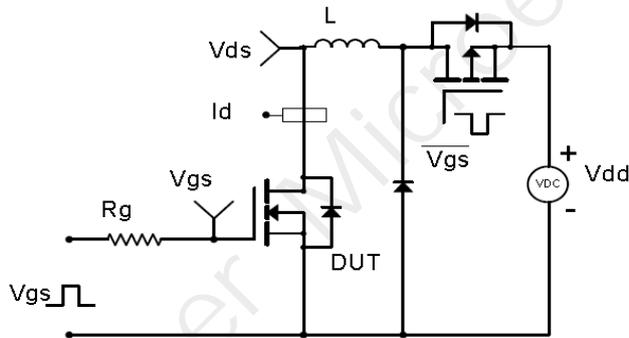
Gate Charge Test Circuit & Waveform



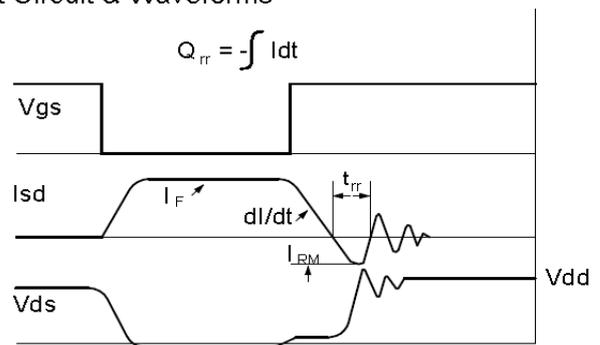
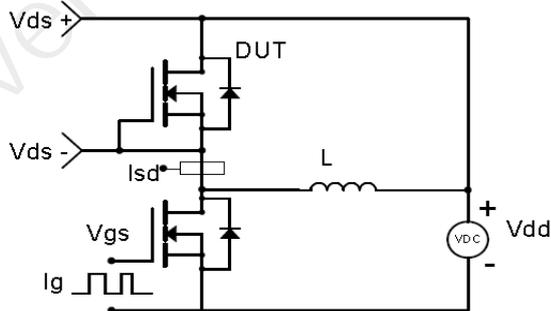
Resistive Switching Test Circuit & Waveforms

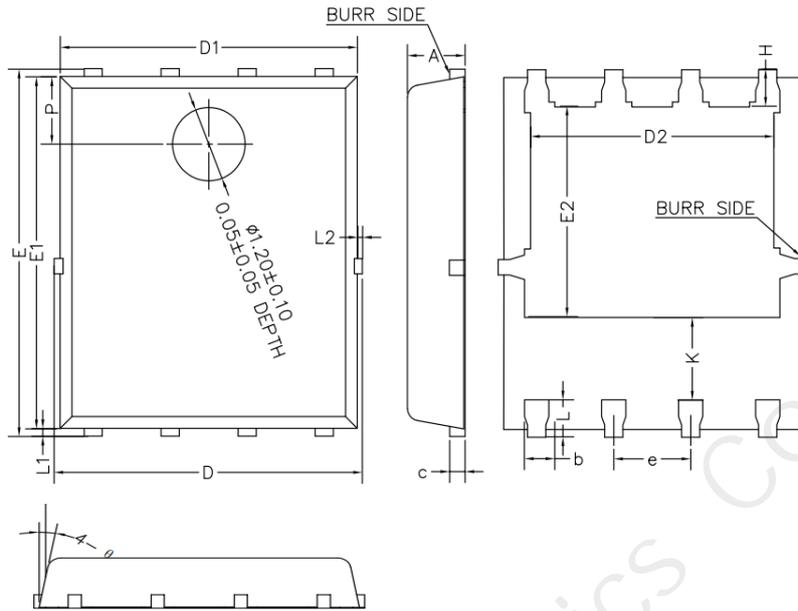


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

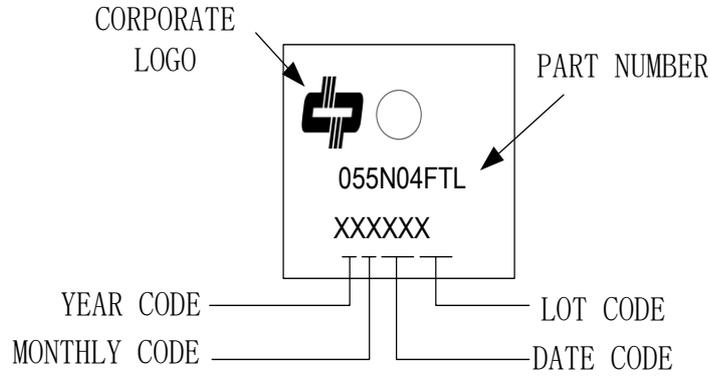


**Package Outline: DFN 5x6**


NOTES:  
DO NOT INCLUDE MOLD FLASH, GATE BURR OR PROTRUSION.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.00	1.20	0.039	0.047
b	0.35	0.45	0.014	0.018
c	0.21	0.34	0.008	0.013
D	-	5.10	-	0.201
D1	4.90	5.00	0.193	0.197
D2	3.91	4.11	0.154	0.162
e	1.17	1.37	0.046	0.054
E	5.90	6.10	0.232	0.240
E1	5.70	5.80	0.224	0.228
E2	3.34	3.54	0.131	0.139
H	0.51	0.71	0.020	0.028
K	1.10	-	0.043	-
L	0.51	0.71	0.020	0.028
L1	0.06	0.20	0.002	0.008
L2	-	0.10	-	0.004
P	1.00	1.10	0.039	0.043
θ	8°	12°	-	-

**Part Marking Information**



Developer Microelectronics Confidential

## Revision History

Revision	Major changes
1.0	Release for formal version

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