

Product Summary

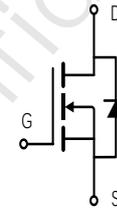
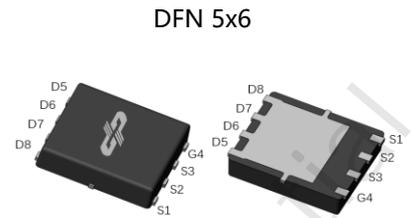
Part #	V _{DS}	R _{DS(on).typ} (@V _{GS} =10V)	R _{DS(on).typ} (@V _{GS} =4.5V)	I _D
DP012N04FGLI	40V	1.15mΩ	1.7mΩ	204A

Features

- Uses advanced DPMOS2 technology
- Better R_{DS(on)} enabled by a low R_{DSon.sp}, low conduction losses
- Excellent Q_gxR_{DS(on)} product(FOM)
- Qualified according to JEDEC criteria

Applications

- Battery management
- Power Management Switches



MSL-1

100% Avalanche Tested

 100% R_g Tested

Package Marking and Ordering Information

Part #	Marking	Package	Packing
DP012N04FGLI	012N04FGLI	DFN 5x6	Tape&Reel


Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V _{DS}	40	V
Continuous drain current	I _D	204	A
T _C = 25°C		129	
T _C = 100°C			
Pulsed drain current (T _C = 25°C, t _p limited by T _{jmax})	I _{D pulse}	816	A
Avalanche energy, single pulse (I=0.3mA, R _g =25) ^[1]	E _{AS}	360	mJ
Gate-Source voltage	V _{GS}	±20	V
Power dissipation (T _C = 25°C)	P _{tot}	96	W
Operating junction and storage temperature	T _j , T _{stg}	-55...+150	°C

 [1].EAS is tested at starting T_j = 25°C, V_{GS} = 10V.

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	1.3	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	52	

Electrical Characteristic (at $T_j = 25\text{ }^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static Characteristic

Drain-source breakdown voltage	BV_{DSS}	40	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{GS(th)}$	1	1.6	2.2	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=40V, V_{GS}=0V$ $T_j=25\text{ }^\circ\text{C}$
		-	-	100		$T_j=150\text{ }^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.15	1.4	mΩ	$T_j=25\text{ }^\circ\text{C}$ $V_{GS}=10V, I_D=40A$
		-	1.7	2.3		$V_{GS}=4.5V, I_D=32A$
Gate resistance	R_g	-	3	-	Ω	$V_{GS}=0V, V_{DS}=0V,$ $f=1\text{MHz}$
Transconductance ^[2]	g_{fs}	-	266	-	S	$V_{DS}=5V, I_D=50A$

Dynamic Characteristic^[2]

Input Capacitance	C_{iss}	-	4163	-	pF	$V_{GS}=0V, V_{DS}=20V,$ $f=1\text{MHz}$
Output Capacitance	C_{oss}	-	1046	-		
Reverse Transfer Capacitance	C_{rss}	-	65	-		
Gate Total Charge($V_{GS}=10V$)	Q_g	-	65	-	nC	$V_{GS}=10V, V_{DS}=20V,$ $I_D=30A, f=1\text{MHz}$
Gate Total Charge($V_{GS}=4.5V$)	Q_g	-	28	-		
Gate-Source charge	Q_{gs}	-	18	-		
Gate-Drain charge	Q_{gd}	-	8	-		
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	$V_{GS}=10V, V_{DD}=20V,$ $R_{G_ext}=2.7\Omega$
Rise time	t_r	-	24	-		
Turn-off delay time	$t_{d(off)}$	-	58	-		
Fall time	t_f	-	59	-		

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.8	1.2	V	$V_{GS}=0V, I_{SD}=40A$
Diode continuous forward current	I_s	-	-	204	A	TC = 25°C
Diode pluse current	$I_{s\ pluse}$	-	-	816	A	TC = 25°C
Body Diode Reverse Recovery Time ^[2]	t_{rr}	-	30	-	ns	$I_F=50A, di/dt=100A/\mu s$
Body Diode Reverse Recovery Charge ^[2]	Q_{rr}	-	15	-	nC	

[2]. Defined by design. Not subject to production test

Typical Performance Characteristics

Fig 1: Output Characteristics

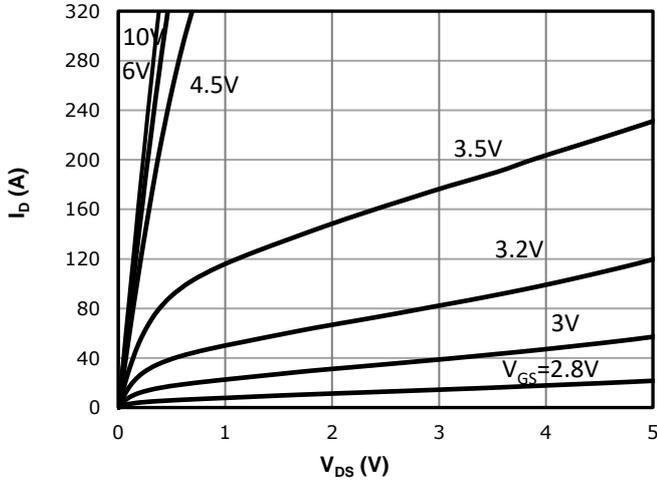


Fig 2: Transfer Characteristics

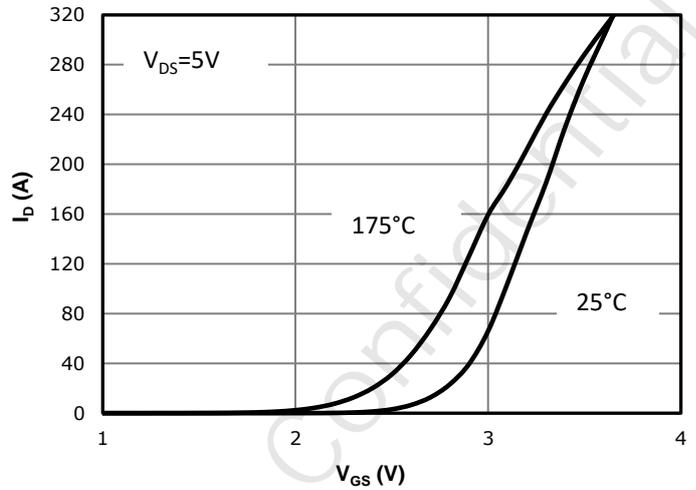


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

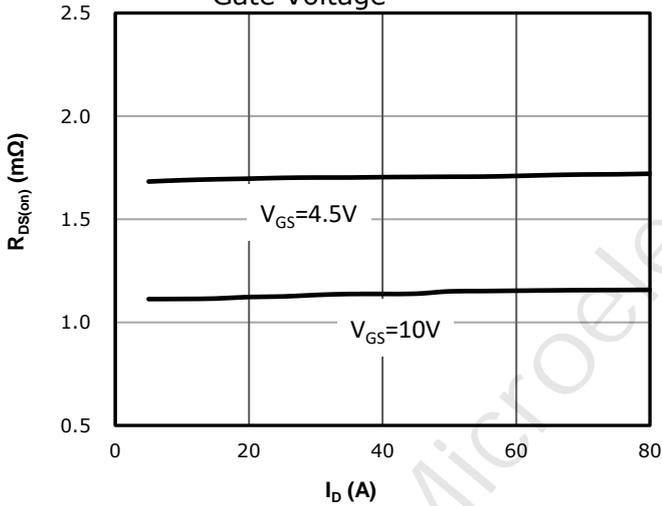


Fig 4: $R_{DS(on)}$ vs Gate Voltage

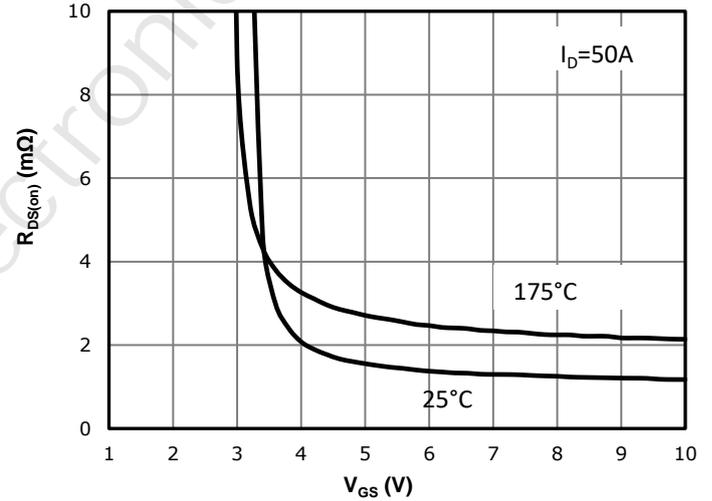


Fig 5: $R_{DS(on)}$ vs. Temperature

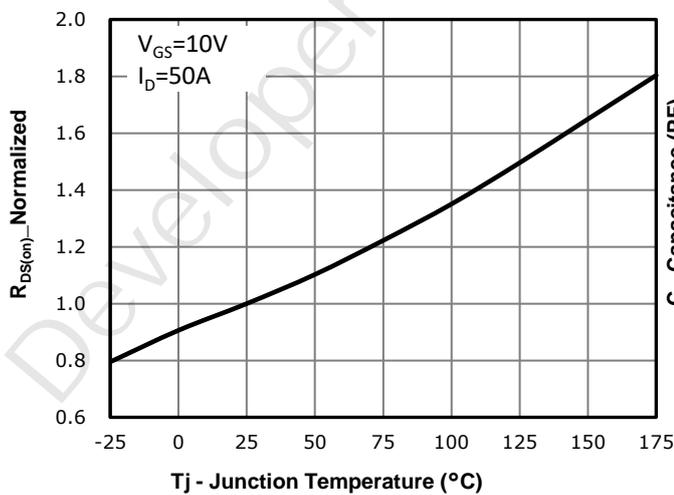


Fig 6: Capacitance Characteristics

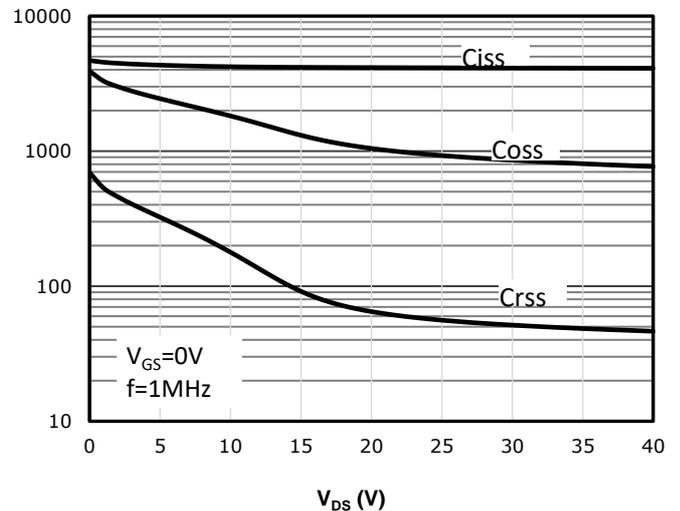


Fig 7: Gate Charge Characteristics

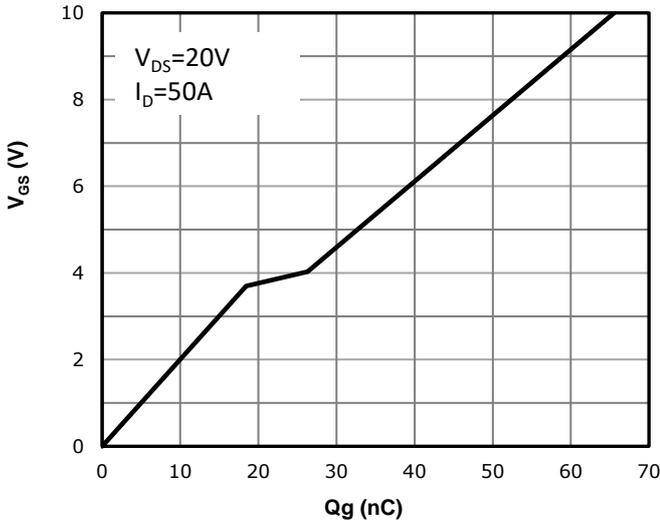


Fig 8: Body-diode Forward Characteristics

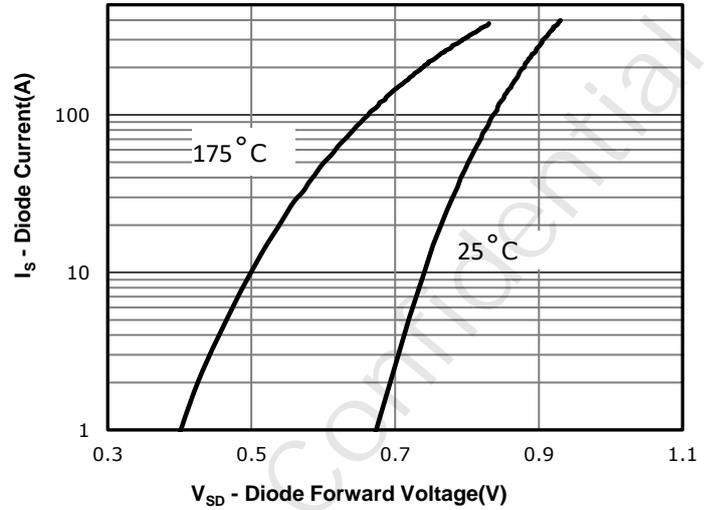


Fig 9: Power Dissipation

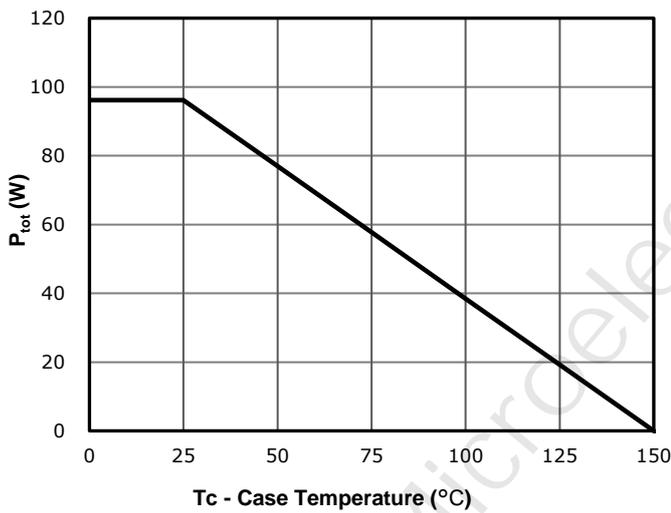


Fig 10: Drain Current Derating

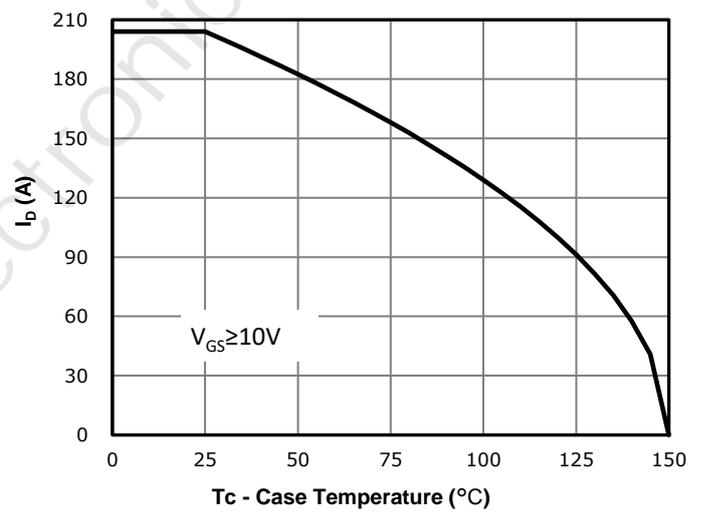


Fig 11: Safe Operating Area

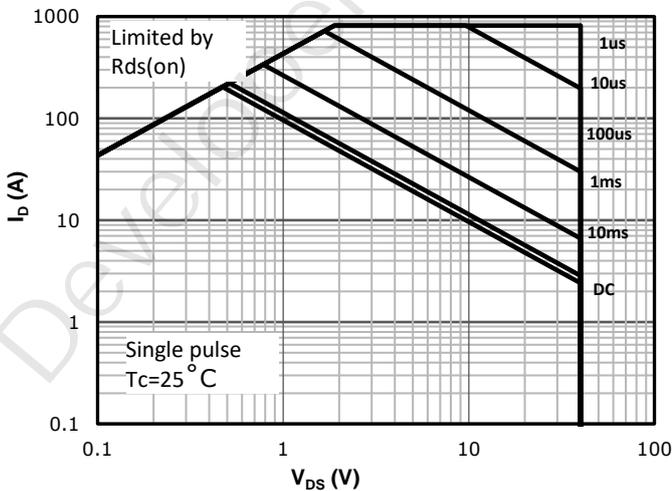
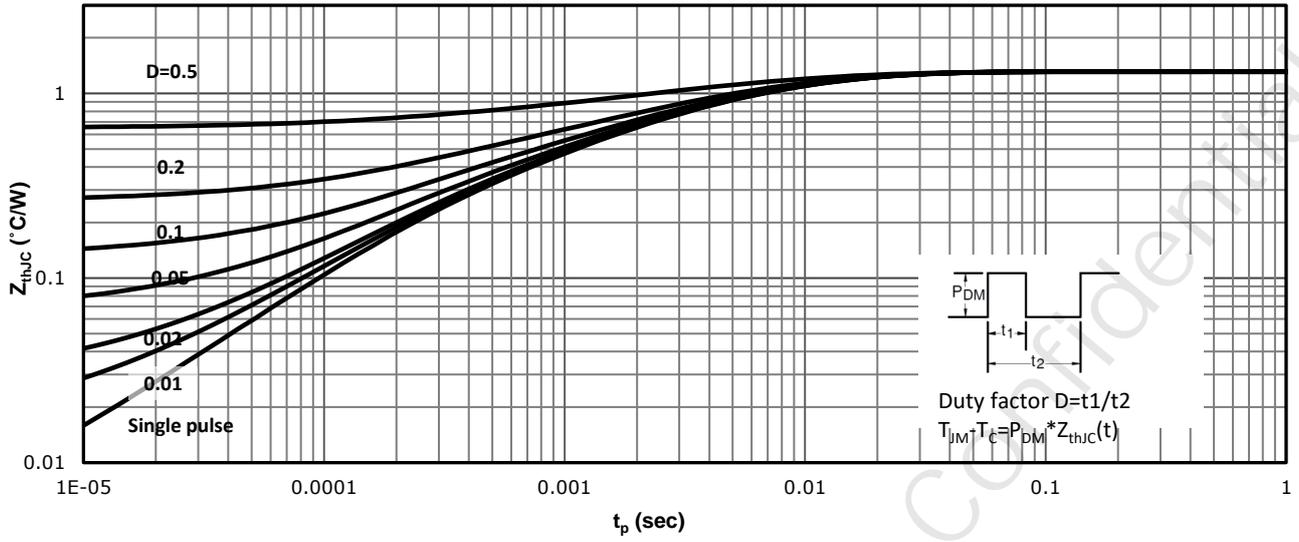
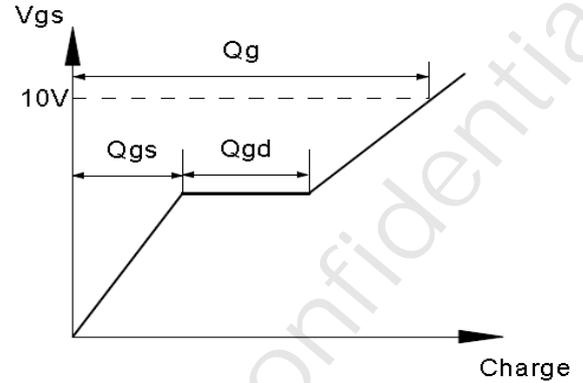
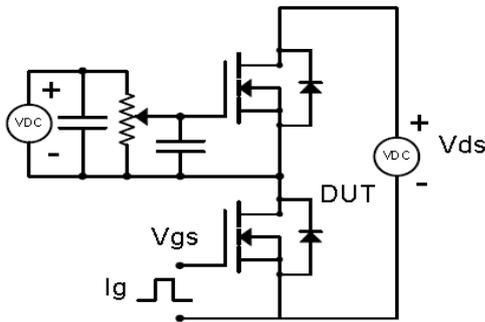


Fig 12: Max. Transient Thermal Impedance

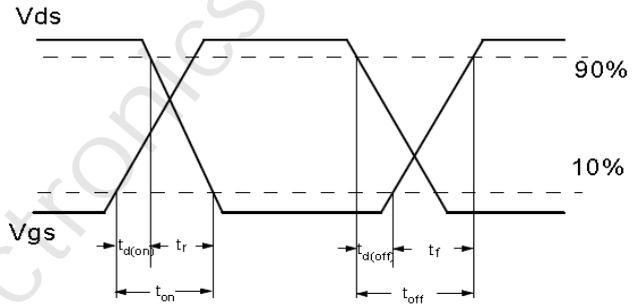
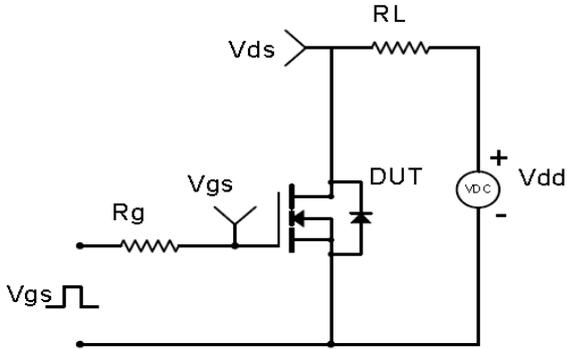


Test Circuit & Waveform

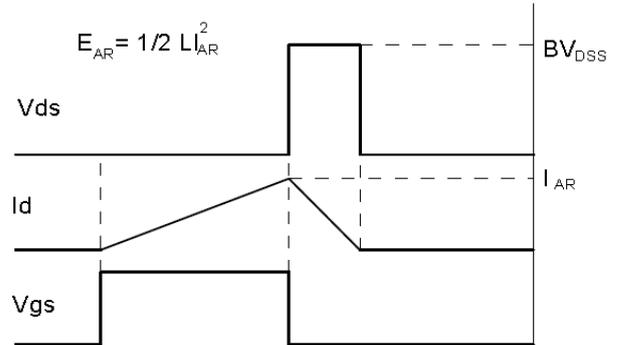
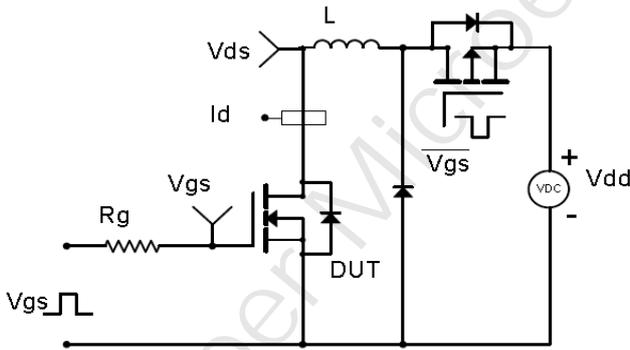
Gate Charge Test Circuit & Waveform



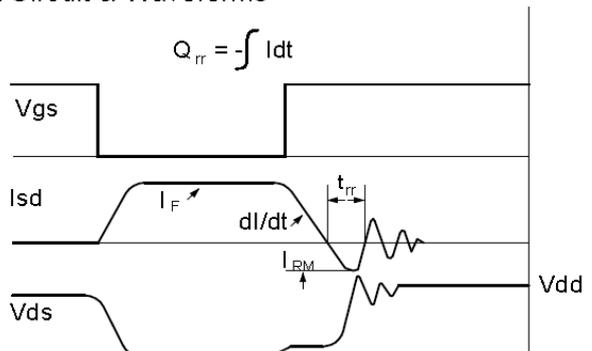
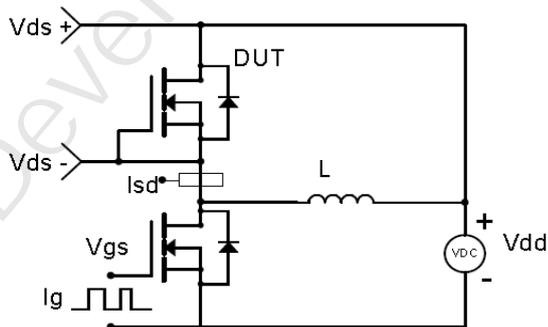
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

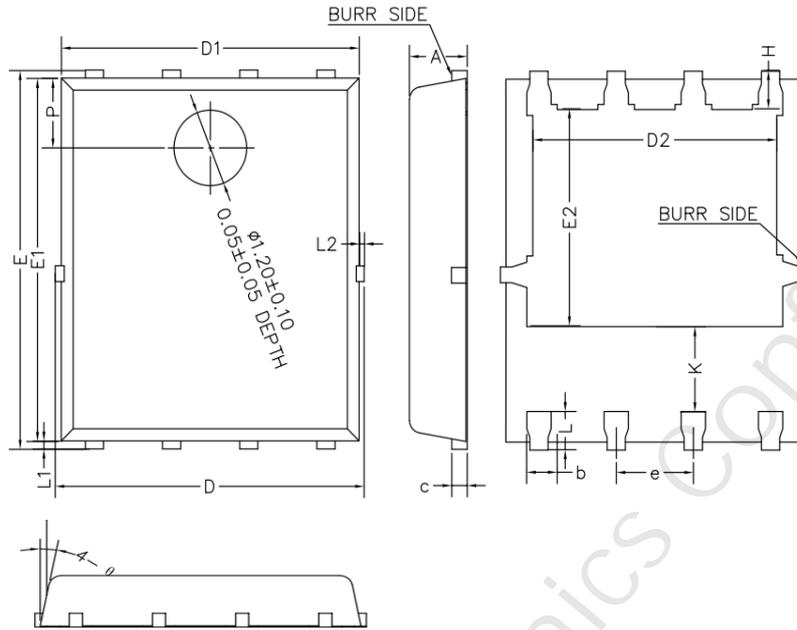


Diode Recovery Test Circuit & Waveforms



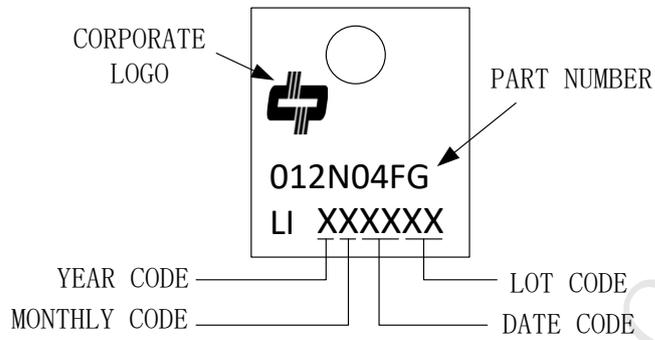


Package Outline: DFN5x6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.00	1.20	0.039	0.047
b	0.35	0.45	0.014	0.018
c	0.21	0.34	0.008	0.013
D	-	5.10	-	0.201
D1	4.90	5.00	0.193	0.197
D2	3.91	4.11	0.154	0.162
e	1.17	1.37	0.046	0.054
E	5.90	6.10	0.232	0.240
E1	5.70	5.80	0.224	0.228
E2	3.34	3.54	0.131	0.139
H	0.51	0.71	0.020	0.028
K	1.10	-	0.043	-
L	0.51	0.71	0.020	0.028
L1	0.06	0.20	0.002	0.008
L2	-	0.10	-	0.004
P	1.00	1.10	0.039	0.043
θ	8°	12°	-	-

Part Marking Information



Developer Microelectronics Confidential

Revision History

Revision	Major changes
1.0	Release for formal version

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