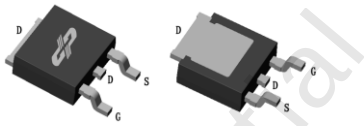
DP7N70D

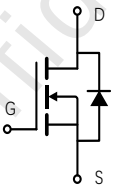
N-MOSFET 700V, 1.3Ω, 7A

Product Summary

Part #	V_{DS}	$R_{DS(on).typ}$	I_D
DP7N70D	700V	1.3Ω	7A

TO-252





100% Avalanche Tested

100% Rg Tested

Features

- Self-aligned planar VDMOS technology
- Low conduction resistance, superior switching performance
- High avalanche energy
- Qualified according to JEDEC criteria

Applications

- Power factor correction
- Charger
- LED Lighting

Package Marking and Ordering Information

Part #	Marking	Package	Packing
DP7N70D	DP7N70D	TO-252	Tape/Reel

Halogen-Free

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	700	V
Continuous drain current T_C = 25°C (Silicon limit) T_C = 100°C (Silicon limit)	I_D	 7 4.6	A
Pulsed drain current (T_C = 25°C, t_p limited by T_{jmax})	$I_{D\ pulse}$	28	A
Avalanche energy, single pulse (L=30mH, Rg=25)[1]	E_{AS}	345	mJ
Peak diode recovery dv/dt[2]	dv/dt	5	V/ns
Gate-Source voltage	V_{GS}	±30	V
Power dissipation (T_C = 25°C)	P_{tot}	48	W
Operating junction and storage temperature	T_j , T_{stg}	-55...+150	°C

[1].EAS is tested at starting T_j = 25℃, V_{GS} = 10V.

[2]. Isd=5A, di/dt<=100A/us, Vdd<=BVds, starting Tj = 25℃

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	2.6	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	62	

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	700	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	V_{DS}=V_{GS},I_D=250uA
Zero gate voltage drain current	I_{DSS}	- -	- -	1 100	μA	V_{DS}=700V,V_{GS}=0V T_j=25°C T_j=125°C(VDS=520V)
Gate-source leakage current	I_{GSS}	-	-	±100	nA	V_{GS}=±30V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.3	1.5	Ω	T_j=25°C V_{GS}=10V, I_D=3.5A
Gate resistance	R_g	-	2	5	Ω	V_{GS}=0V, V_{DS}=0V, f=1MHz
Transconductance[2]	g_{fs}	-	15	-	S	V_{DS}=15V,I_D=8A
Dynamic Characteristic[3]						
Input Capacitance	C_{iss}	-	1193	-	pF	V_{GS}=0V, V_{DS}=40V, f=1MHz
Output Capacitance	C_{oss}	-	90	-		
Reverse Transfer Capacitance	C_{rss}	-	10	-		
Gate Total Charge(V_{GS}=10V)	Q_g	-	20	-	nC	V_{GS}=10V, V_{DS}=560V, I_D=5A, f=1MHz
Gate-Source charge	Q_{gs}	-	5	-		
Gate-Drain charge	Q_{gd}	-	8	-		
Turn-on delay time	$t_{d(on)}$	-	26	-	ns	V_{GS}=10V, V_{DD}=350V, R_{G_ext}=10Ω
Rise time	t_r	-	48	-		
Turn-off delay time	$t_{d(off)}$	-	57	-		
Fall time	t_f	-	33	-		

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.8	1.2	V	V_{GS}=0V,I_{SD}=7A
Diode continuous forward current	I_s	-	-	7	A	TC = 25°C
Diode pluse current	$I_{s\ pluse}$	-	-	28	A	TC = 25°C
Body Diode Reverse Recovery Time[3]	t_{rr}	-	271	-	ns	I_F=7A, dI/dt=100A/μs
Body Diode Reverse Recovery Charge[3]	Q_{rr}	-	4	-	uC	

[3]. Defined by design. Not subject to production test

Typical Performance Characteristics

Fig 1: Output Characteristics

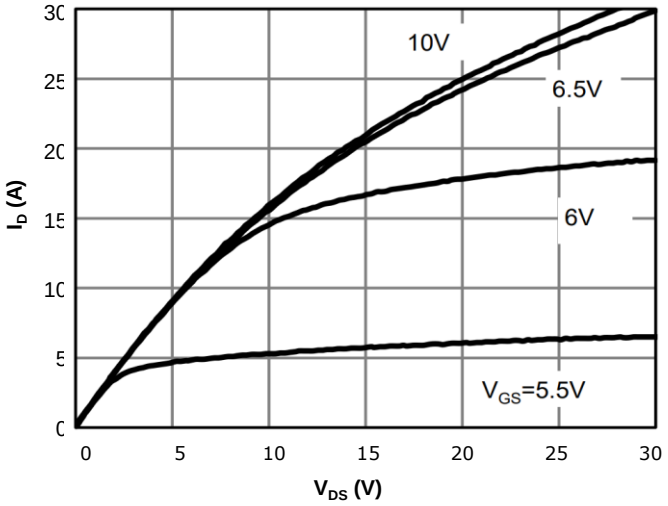


Fig 2: Transfer Characteristics

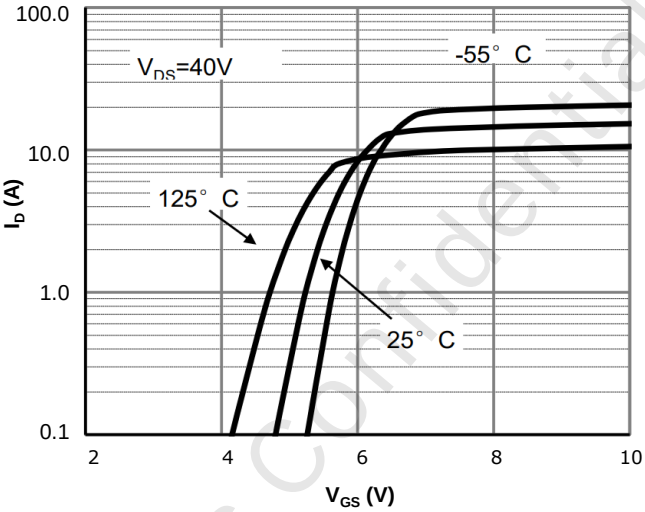


Fig 3: Rds(on) vs Drain Current and Gate Voltage

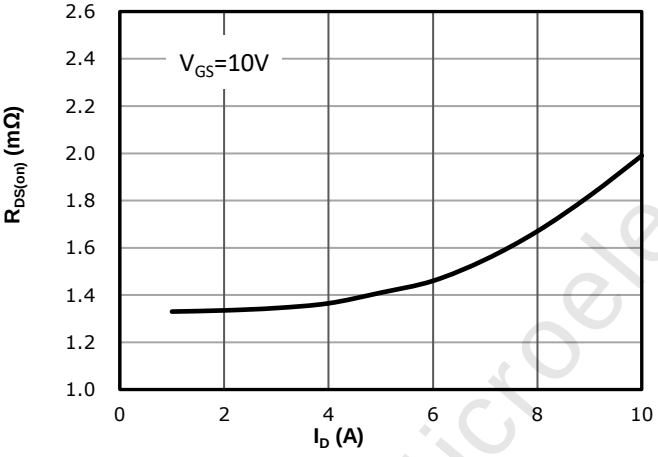


Fig 4: Break Down vs. Junction Temperature

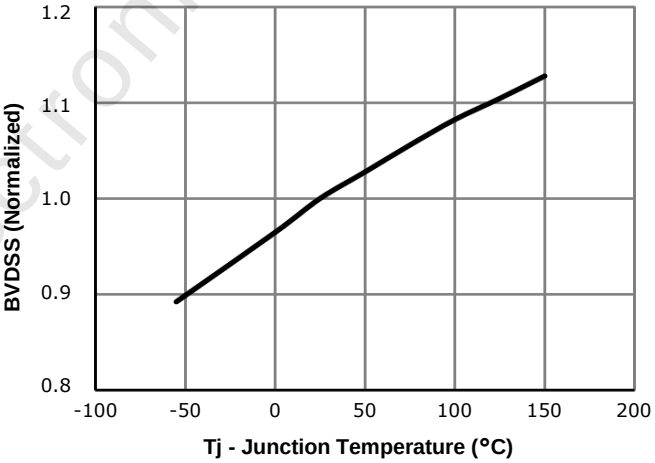


Fig 5: Rds(on) vs. Temperature

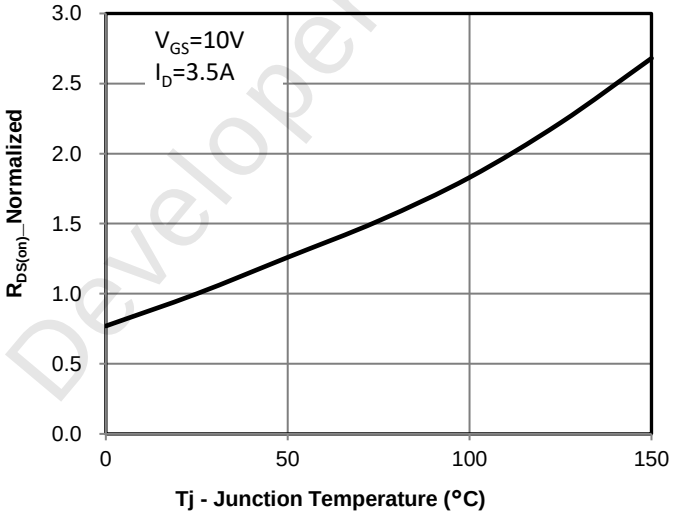


Fig 6: Capacitance Characteristics

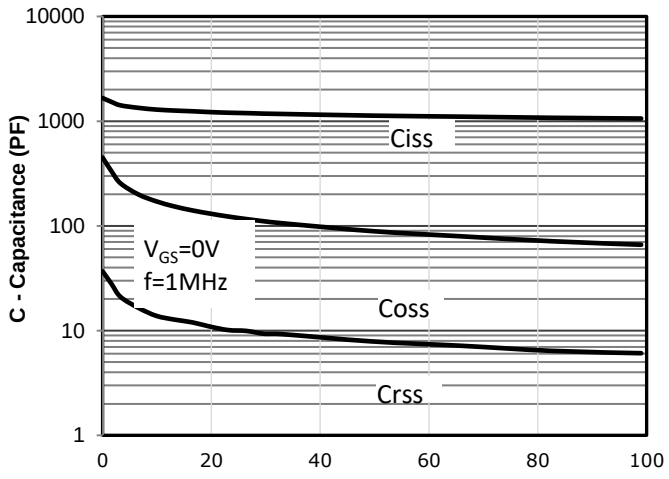


Fig 7: Gate Charge Characteristics

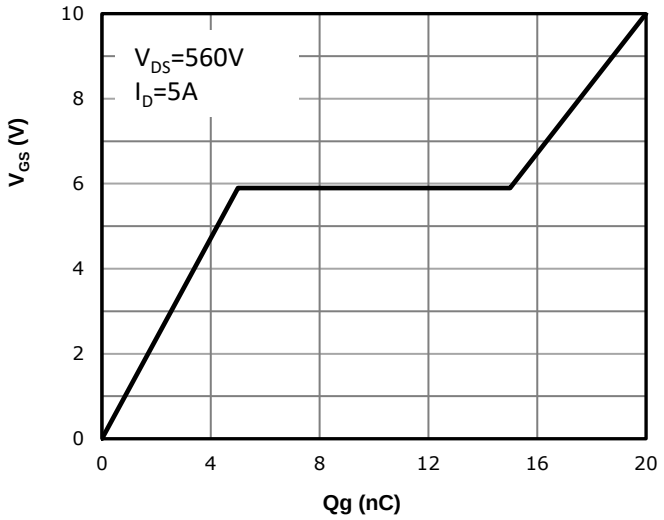


Fig 8: Body-diode Forward Characteristics

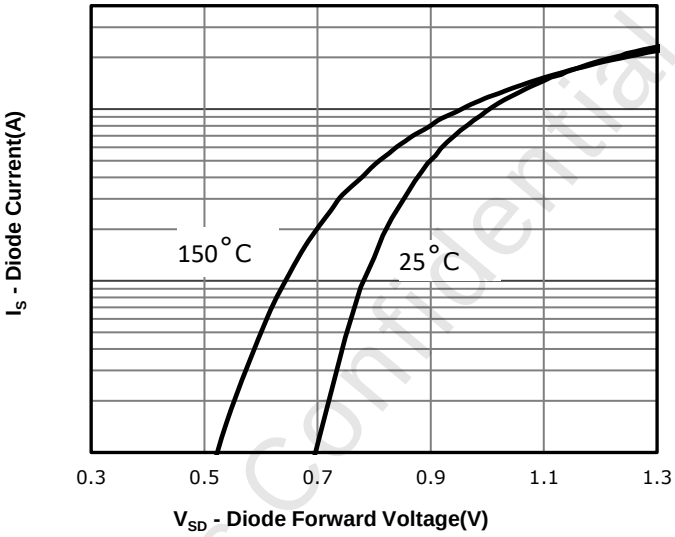


Fig 9: Power Dissipation

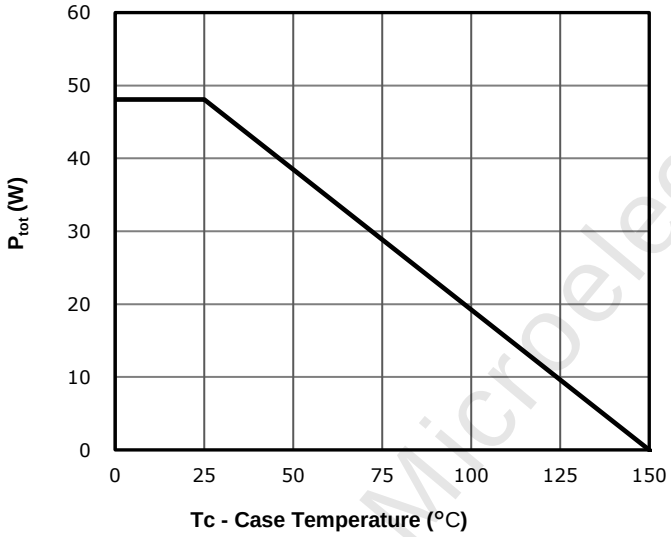


Fig 10: Drain Current Derating

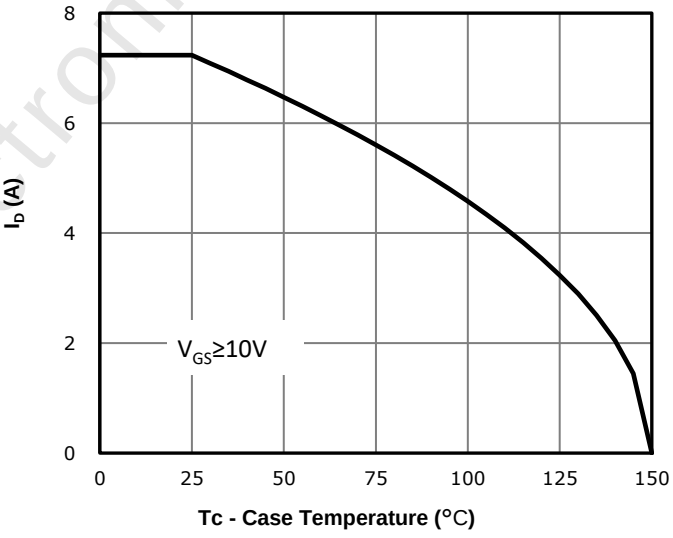


Fig 11: Safe Operating Area

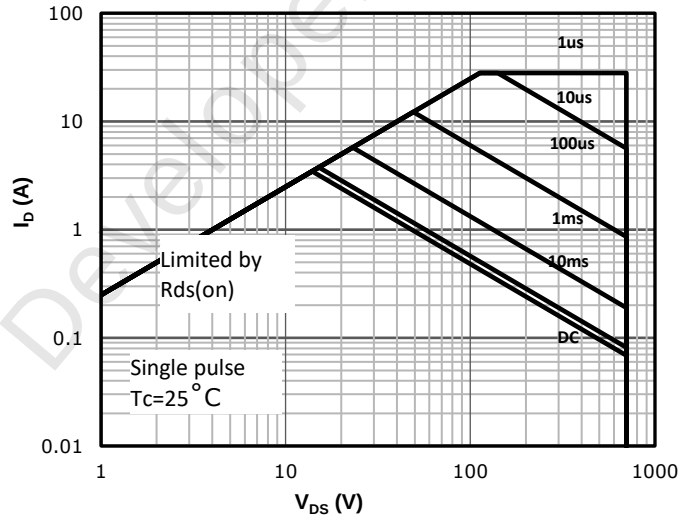
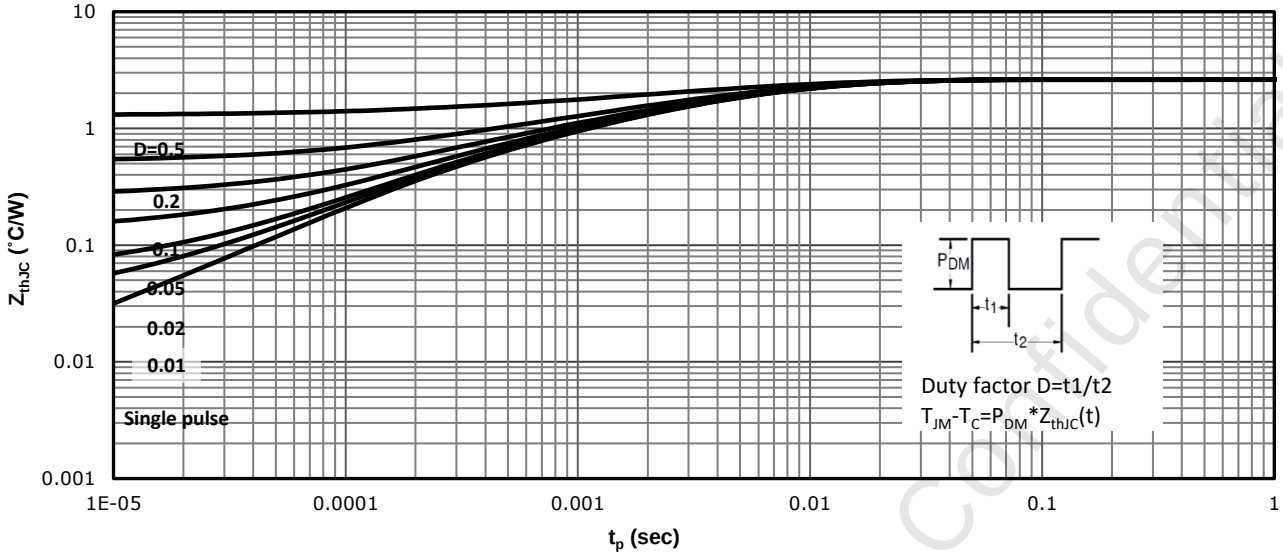
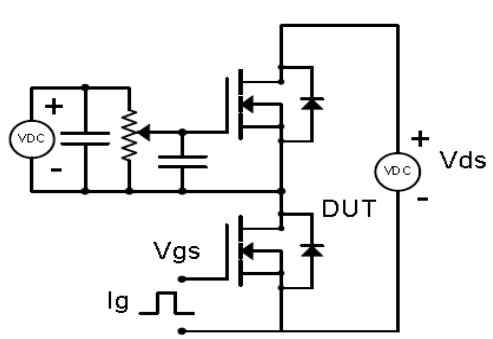


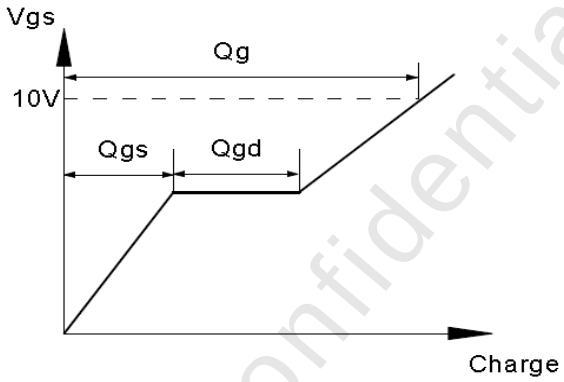
Fig 12: Max. Transient Thermal Impedance



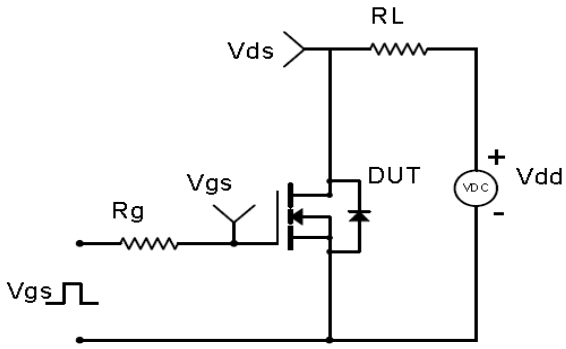
Test Circuit & Waveform

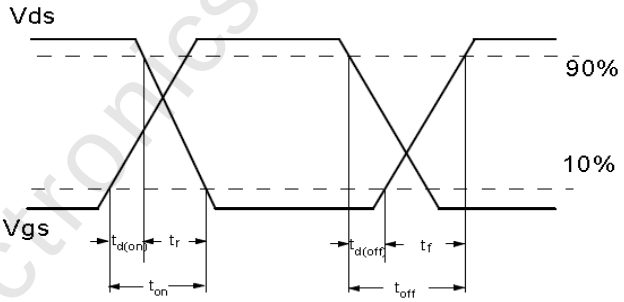
Gate Charge Test Circuit & Waveform



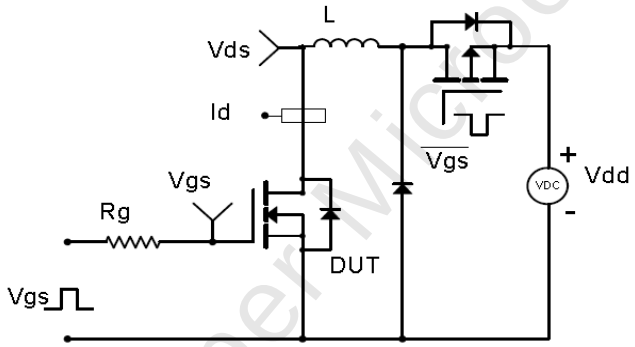


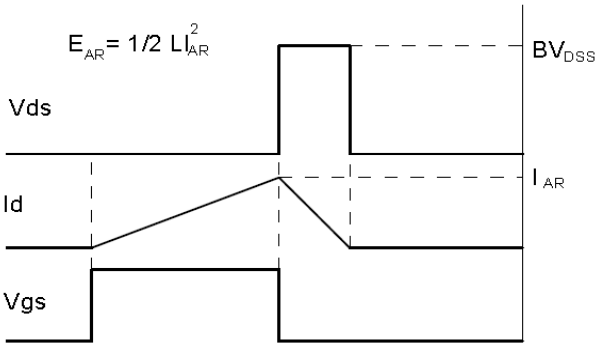
Resistive Switching Test Circuit & Waveforms



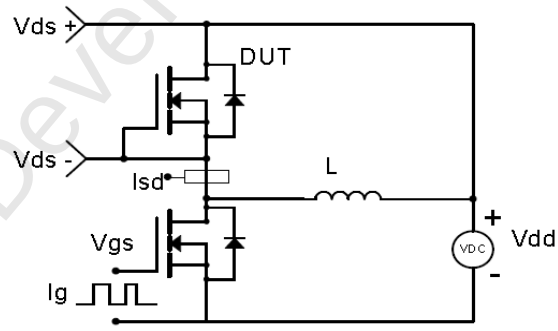


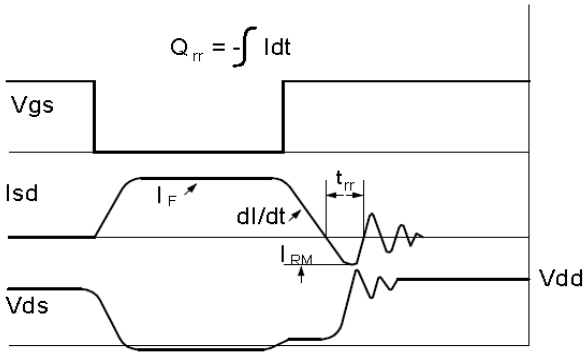
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



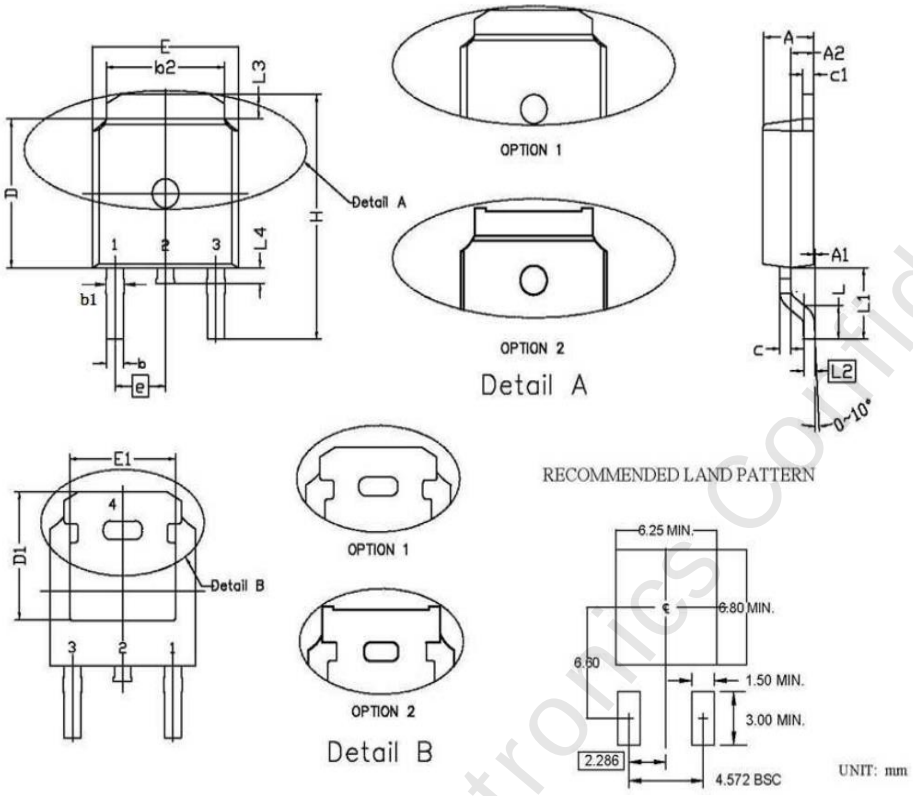


Diode Recovery Test Circuit & Waveforms



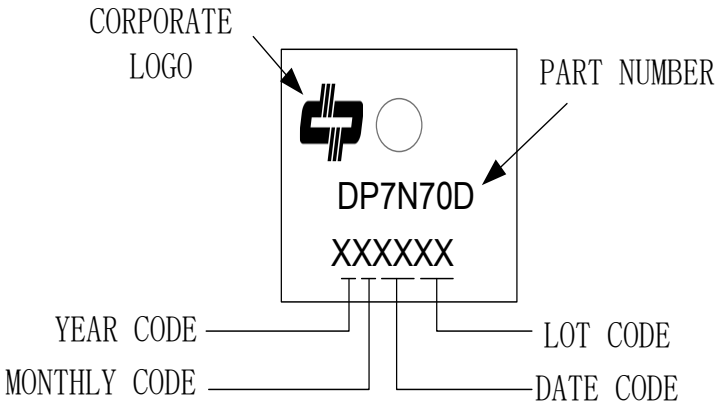


Package Outline: TO-252



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.15	2.45	0.085	0.096
A1	0.00	0.15	0.000	0.006
A2	0.76	1.36	0.030	0.054
b	0.60	0.91	0.024	0.036
b1	0.65	1.15	0.026	0.045
b2	5.00	5.64	0.197	0.222
c	0.45	0.61	0.018	0.024
c1	0.36	0.66	0.014	0.026
D	5.80	6.30	0.228	0.248
D1	5.00	6.00	0.197	0.236
e	2.29 BSC.		0.090 BSC.	
E	6.30	6.90	0.248	0.272
E1	4.55	5.30	0.179	0.209
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L1	2.92 REF		0.115 REF	
L2	0.36	0.66	0.014	0.026
L3	0.72	1.35	0.028	0.053
L4	0.60	1.20	0.024	0.047

Part Marking Information



Revision History

Revison	Major changes
1.0	Release for formal version

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