

Product Summary

Part #	V _{DS}	R _{DS(on).typ} (@V _{GS} =10V)	R _{DS(on).typ} (@V _{GS} =4.5V)	I _D
DP032N10FGL2I	100V	2.4mΩ	3mΩ	205A

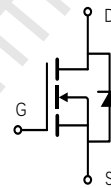
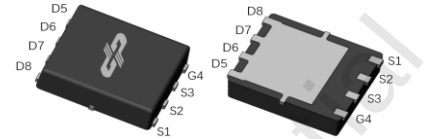
Features

- Uses advanced MOSFET-DPMOS2 technology
- Extremely low on-resistance R_{DS(on)}
- Excellent Q_gxR_{DS(on)} product(FOM)
- Qualified according to JEDEC criteria

Applications

- Motor control and drive
- Battery management
- UPS (Uninterruptible Power Supplies)

DFN 5x6



MSL level1

100% Avalanche Tested

100% R_g Tested

Package Marking and Ordering Information

Part #	Marking	Package	Packing
DP032N10FGL2I	032N10FGL2I	DFN5x6	Tape&Reel



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V _{DS}	100	V
Continuous drain current T _C = 25°C (Silicon limit) T _C = 100°C (Silicon limit)	I _D	205 145	A
Pulsed drain current (T _C = 25°C, t _p limited by T _{jmax})	I _D pulse	820	A
Avalanche energy, single pulse (L=0.5mH, R _g =25Ω) ^[1]	E _{AS}	361	mJ
Gate-Source voltage	V _{GS}	±20	V
Power dissipation (T _C = 25°C)	P _{tot}	213	W
Operating junction and storage temperature	T _j , T _{stg}	-55...+175	°C

[1].EAS is tested at starting T_j = 25°C, V_{GS} = 10V.

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	0.7	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	50	

Electrical Characteristic (at $T_j = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static Characteristic

Drain-source breakdown voltage	BV_{DSS}	100	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.2	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1 100	μA	$V_{DS}=100V, V_{GS}=0V$ $T_j=25^\circ\text{C}$ $T_j=125^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.4 3.0	3.0 3.9	mΩ	$V_{GS}=10V, I_D=40A$ $V_{GS}=4.5V, I_D=40A$
Gate resistance	R_g	-	2.4	-	Ω	$V_{GS}=0V, V_{DS}=0V,$ $f=1\text{MHz}$
Transconductance ^[2]	g_{fs}	-	100	-	S	$V_{DS}=5V, I_D=20A$

Dynamic Characteristic^[2]

Input Capacitance	C_{iss}	-	4436	-	pF	$V_{GS}=0V, V_{DS}=50V,$ $f=1\text{MHz}$
Output Capacitance	C_{oss}	-	1977	-		
Reverse Transfer Capacitance	C_{rss}	-	32	-		
Gate Total Charge	Q_g	-	65	-	nC	$V_{GS}=10V, V_{DS}=50V,$ $I_D=50A, f=1\text{MHz}$
Gate-Source charge	Q_{gs}	-	19	-		
Gate-Drain charge	Q_{gd}	-	9	-		
Turn-on delay time	$t_{d(on)}$	-	15	-	ns	$V_{GS}=10V, V_{DD}=50V,$ $R_{G_ext}=2.7\Omega$
Rise time	t_r	-	47	-		
Turn-off delay time	$t_{d(off)}$	-	46	-		
Fall time	t_f	-	18	-		

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.8	1.3	V	$V_{GS}=0V, I_{SD}=20A$
Diode continuous forward current	I_s	-	-	205	A	TC = 25°C
Diode pluse current	$I_{s\ pluse}$	-	-	820	A	TC = 25°C
Body Diode Reverse Recovery Time ^[2]	t_{rr}	-	58	-	ns	$I_F=50A, dI/dt=40A/\mu s$
Body Diode Reverse Recovery Charge ^[2]	Q_{rr}	-	95	-	nC	

[2]. Defined by design. Not subject to production test

Typical Performance Characteristics

Fig 1: Output Characteristics

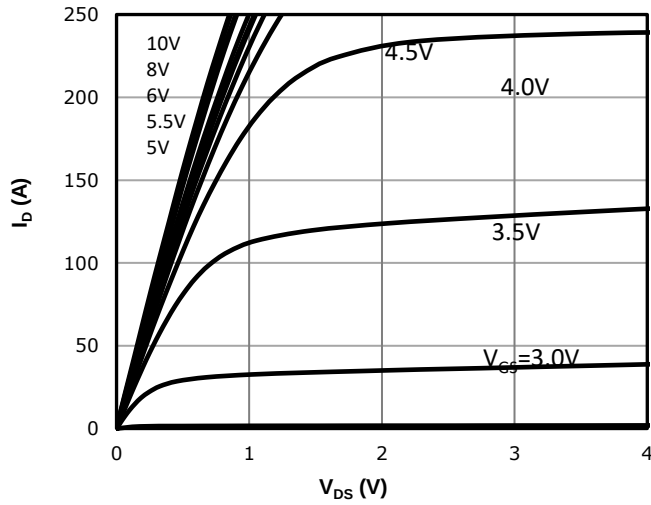


Fig 2: Transfer Characteristics

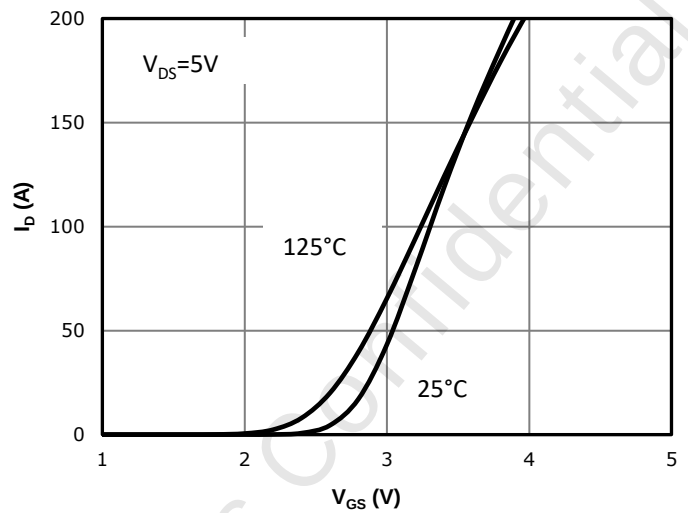


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

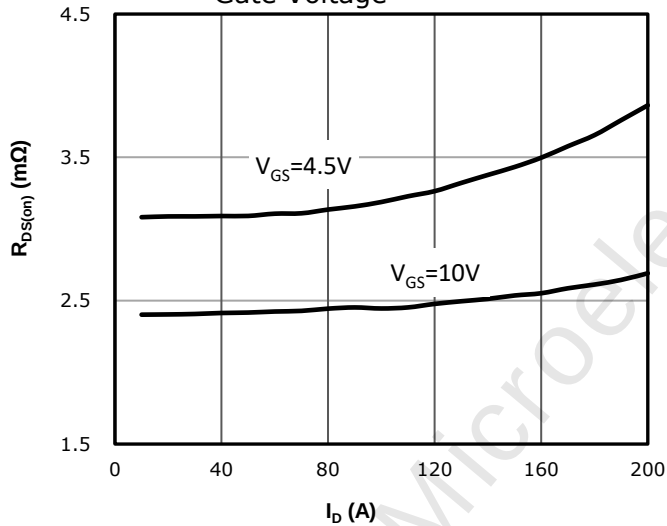


Fig 4: $R_{DS(on)}$ vs Gate Voltage

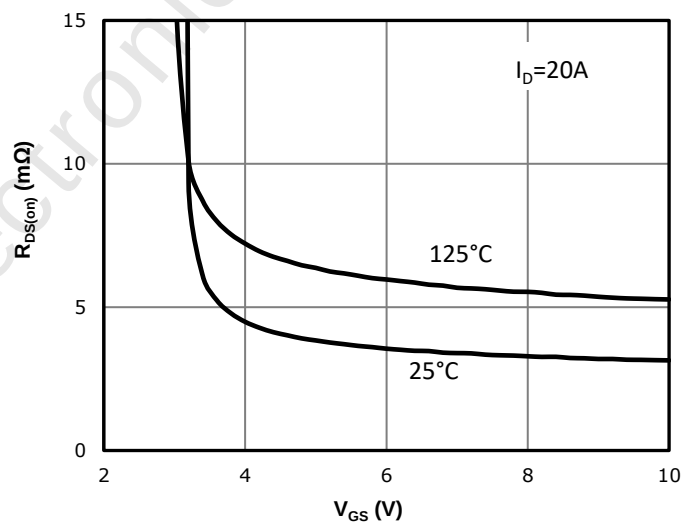


Fig 5: $R_{DS(on)}$ vs. Temperature

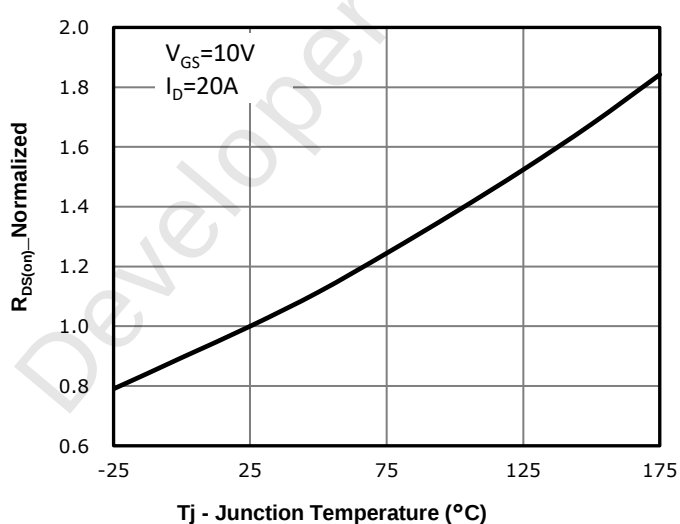


Fig 6: Capacitance Characteristics

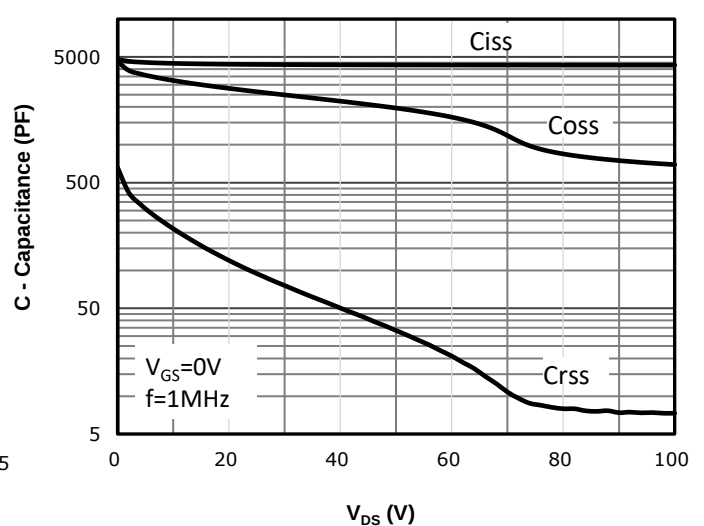


Fig 7: Gate Charge Characteristics

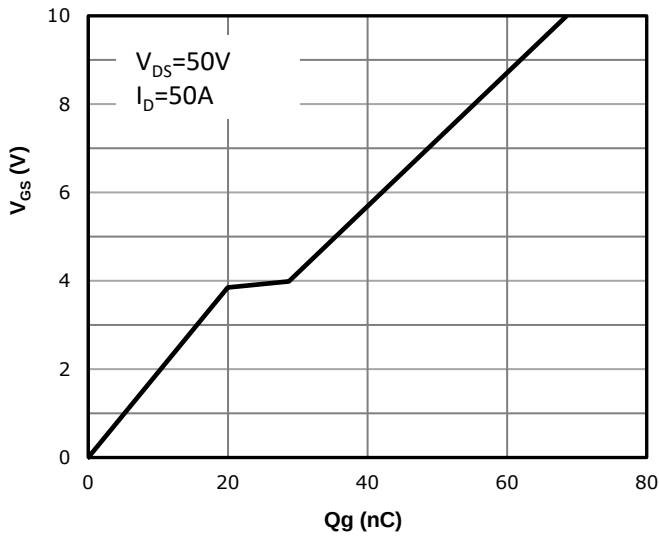


Fig 8: Body-diode Forward Characteristics

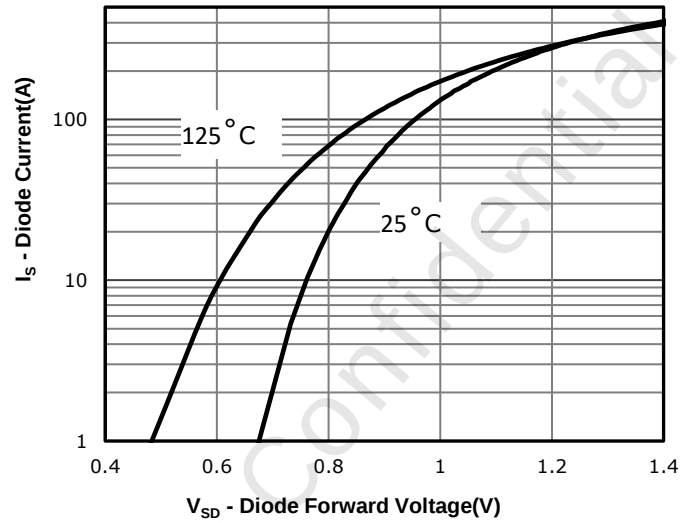


Fig 9: Power Dissipation

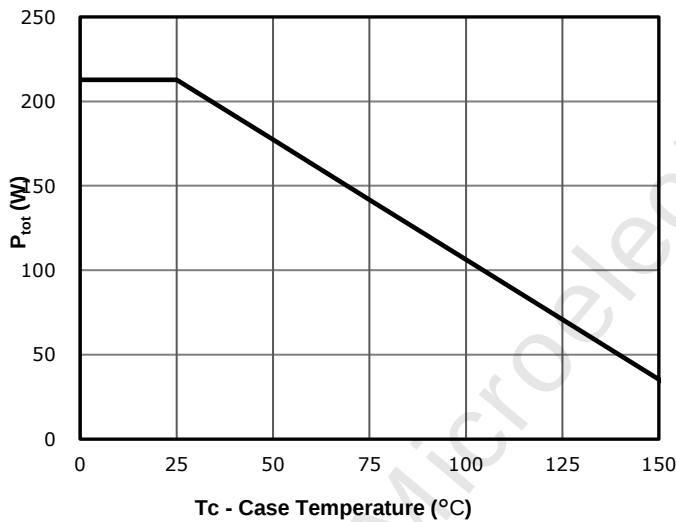


Fig 10: Drain Current Derating

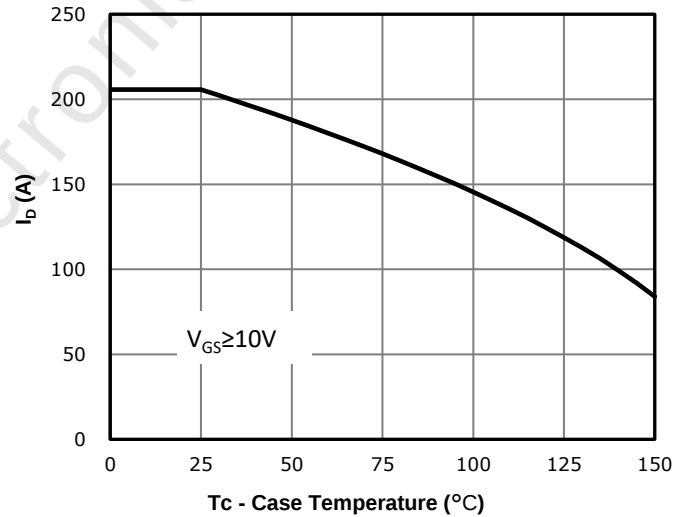


Fig 11: Safe Operating Area

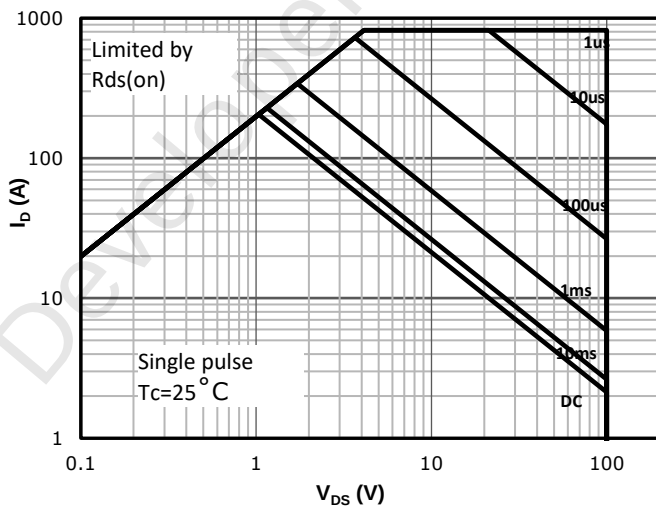
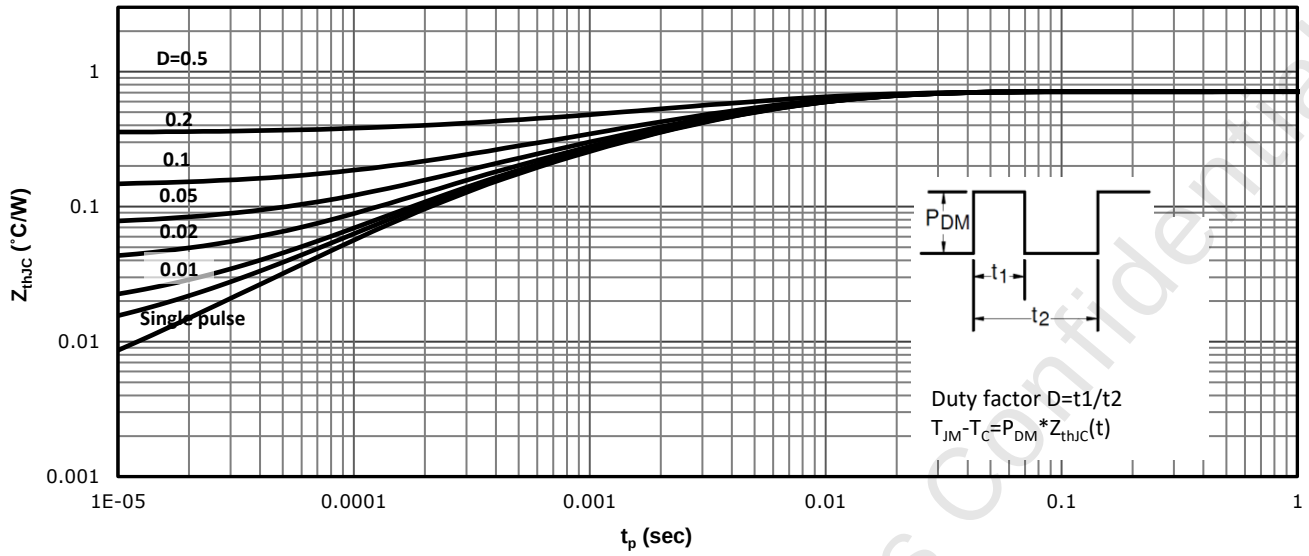
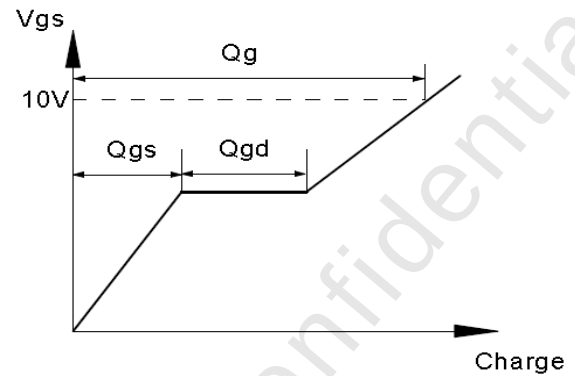
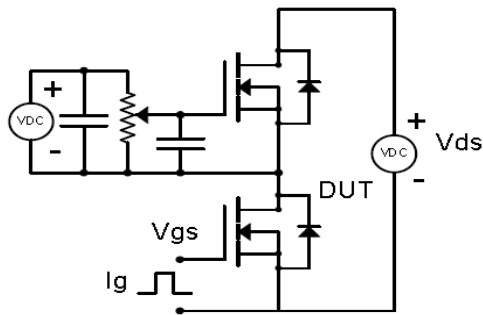


Fig 12: Max. Transient Thermal Impedance

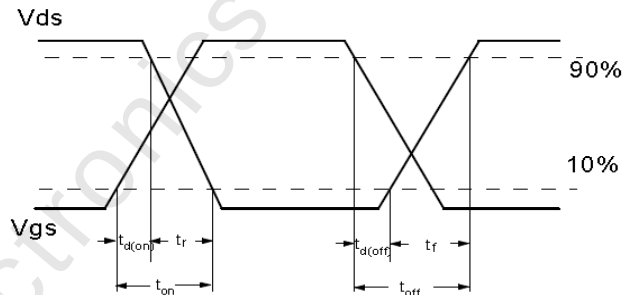
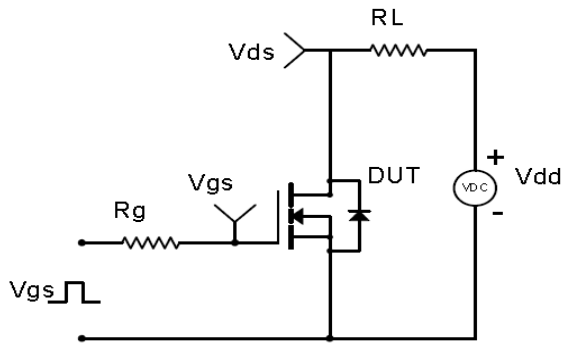


Test Circuit & Waveform

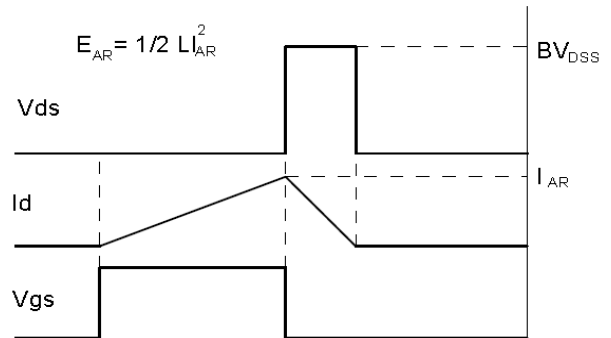
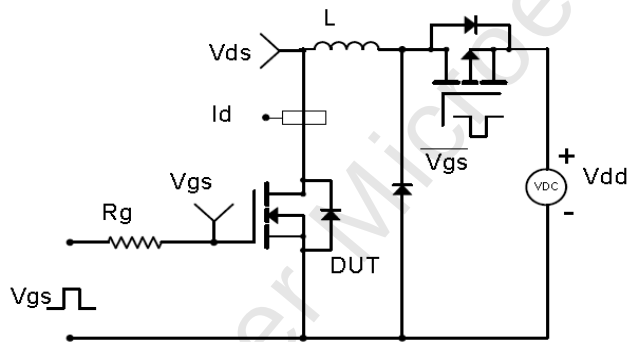
Gate Charge Test Circuit & Waveform



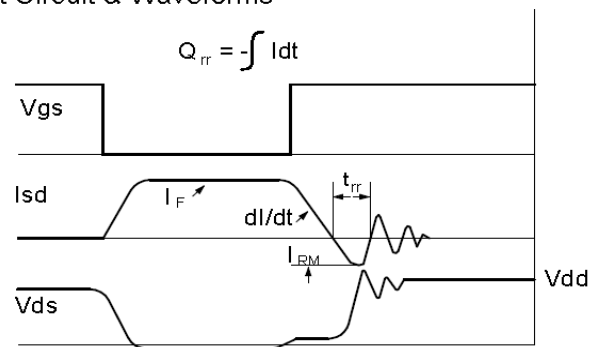
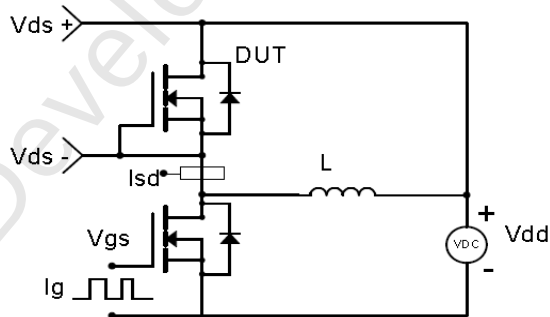
Resistive Switching Test Circuit & Waveforms



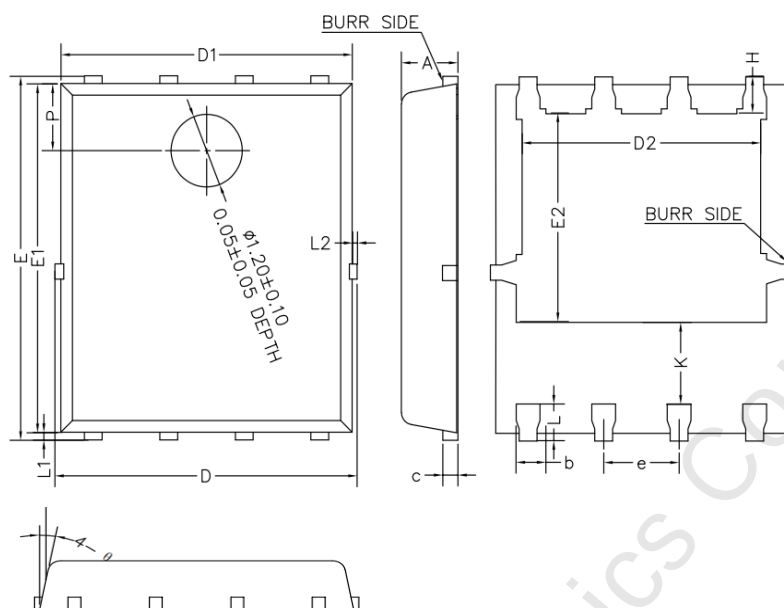
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



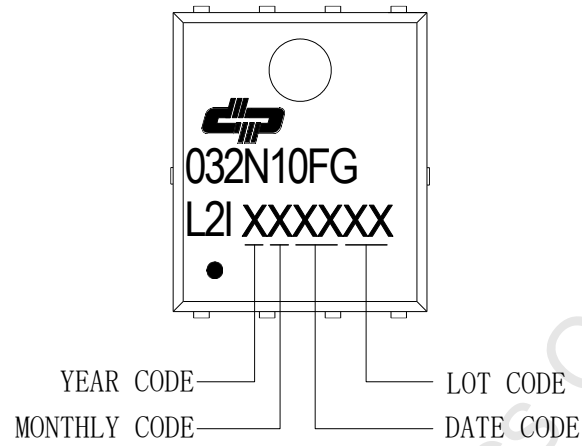
Package Outline: DFN5x6



NOTES:
DO NOT INCLUDE MOLD FLASH,GATE BURR OR PROTRUSION.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.00	1.20	0.039	0.047
b	0.35	0.45	0.014	0.018
c	0.21	0.34	0.008	0.013
D	-	5.10	-	0.201
D1	4.90	5.00	0.193	0.197
D2	3.91	4.11	0.154	0.162
e	1.17	1.37	0.046	0.054
E	5.90	6.10	0.232	0.240
E1	5.70	5.80	0.224	0.228
E2	3.34	3.54	0.131	0.139
H	0.51	0.71	0.020	0.028
K	1.10	-	0.043	-
L	0.51	0.71	0.020	0.028
L1	0.06	0.20	0.002	0.008
L2	-	0.10	-	0.004
P	1.00	1.10	0.039	0.043
θ	8°	12°	-	-

Part Marking Information



Revision History

Revision	Major changes
1.0	Release for formal version

重要声明Important Notice

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