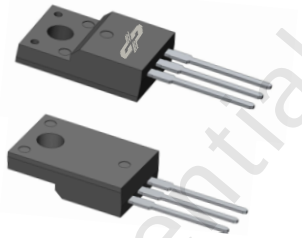
DP70R280AJ

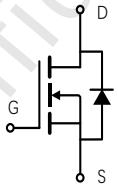
SJ N-MOSFET 700V, 0.22Ω, 15A

Product Summary

Part #	V_{DS}	$R_{DS(on).typ}$	I_D
DP70R280AJ	700V	0.22Ω	15A

TO-220F





100% Avalanche Tested

100% Rg Tested

Features

- Super_Junction technology
- Low conduction resistance, superior switching performance
- High avalanche energy
- Better efficiency due to very low FOM

Applications

- Power factor correction
- Charger
- LED Lighting

Package Marking and Ordering Information

Part #	Marking	Package	Packing
DP70R280AJ	70R280AJ	TO-220F	Tube

Halogen-Free

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	700	V
Continuous drain current T_C = 25°C T_C = 100°C	I_D	 15 9.6	A
Pulsed drain current (T_C = 25°C, t_p limited by T_{jmax})	$I_{D\ pulse}$	45	A
Avalanche energy, single pulse (L=10mH, Rg=25)[1]	E_{AS}	80	mJ
Peak diode recovery dv/dt[2]	dv/dt	50	V/ns
Gate-Source voltage	V_{GS}	±30	V
Power dissipation (T_C = 25°C)	P_{tot}	37	W
Operating junction and storage temperature	T_j , T_{stg}	-55...+150	°C

[1].EAS is tested at starting T_j = 25°C, V_{GS} = 10V.

[2]. Identical low side and high side switch with identical Rg

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Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	3.4	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	62	

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	700	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{GS(th)}$	3	3.6	4.2	V	V_{DS}=V_{GS},I_D=250uA
Zero gate voltage drain current	I_{DSS}	- -	- -	1 100	μA	V_{DS}=700V,V_{GS}=0V T_j=25°C T_j=125°C(VDS=560V)
Gate-source leakage current	I_{GSS}	-	-	±100	nA	V_{GS}=±30V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.22	0.28	Ω	T_j=25°C VGS=10V, ID=7.5A
Gate resistance	R_g	-	4	-	Ω	V_{GS}=0V, V_{DS}=0V, f=1MHz
Transconductance[2]	g_{fs}	-	11	-	S	VDS=20V,ID=6A
Dynamic Characteristic[3]						
Input Capacitance	C_{iss}	-	1321	-	pF	V_{GS}=0V, V_{DS}=40V, f=1MHz
Output Capacitance	C_{oss}	-	306	-		
Reverse Transfer Capacitance	C_{rss}	-	7.6	-		
Gate Total Charge(V_{GS}=10V)	Q_g	-	32	-	nC	VGS=10V, VDS=560V, ID=7.5A, f=1MHz
Gate-Source charge	Q_{gs}	-	6.8	-		
Gate-Drain charge	Q_{gd}	-	12	-		
Turn-on delay time	$t_{d(on)}$	-	24	-	ns	V_{GS}=10V, V_{DD}=400V, R_{G_ext}=10Ω
Rise time	t_r	-	31	-		
Turn-off delay time	$t_{d(off)}$	-	78	-		
Fall time	t_f	-	9	-		

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Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.8	1.1	V	VGS=0V,ISD=7.5A
Diode continuous forward current	I_s	-	-	15	A	TC = 25°C
Diode pluse current	$I_{s\ pluse}$	-	-	45	A	TC = 25°C
Body Diode Reverse Recovery Time[3]	t_{rr}	-	272	-	ns	IF=7.5A, dI/dt=100A/μs
Body Diode Reverse Recovery Charge[3]	Q_{rr}	-	2.8	-	uC	

[3]. Defined by design. Not subject to production test

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Typical Performance Characteristics

Fig 1: Output Characteristics

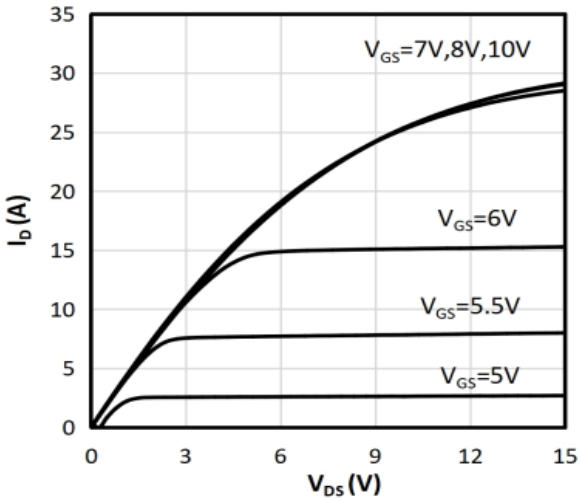


Fig 2: Transfer Characteristics

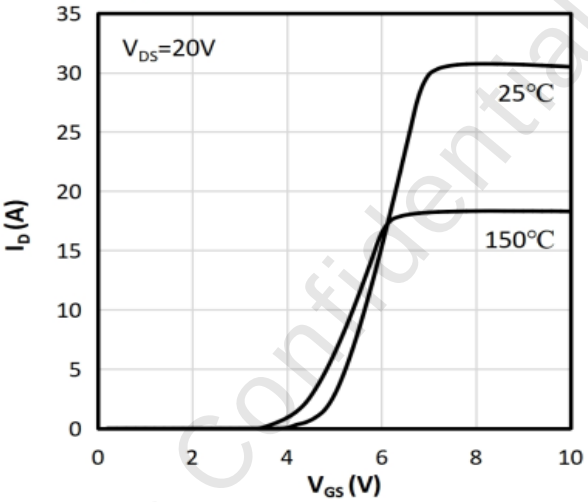


Fig 3: Rds(on) vs Drain Current

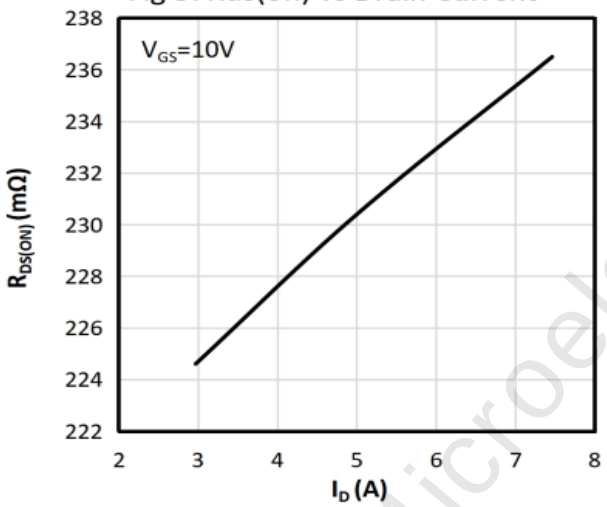


Fig 4: Rds(on) vs. Temperature

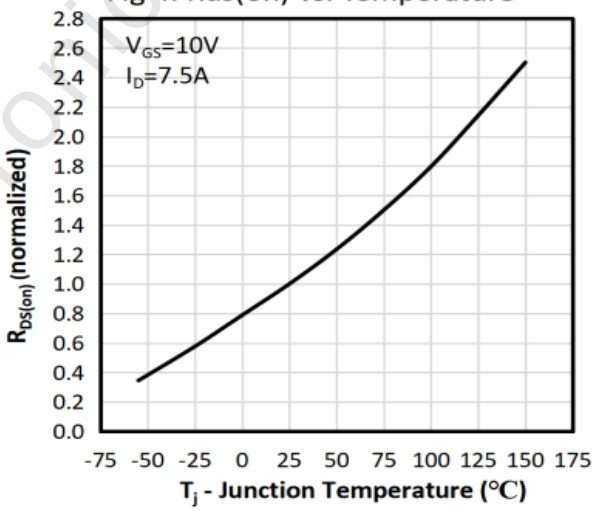


Fig 5: Breakdown Voltage vs. Temperature

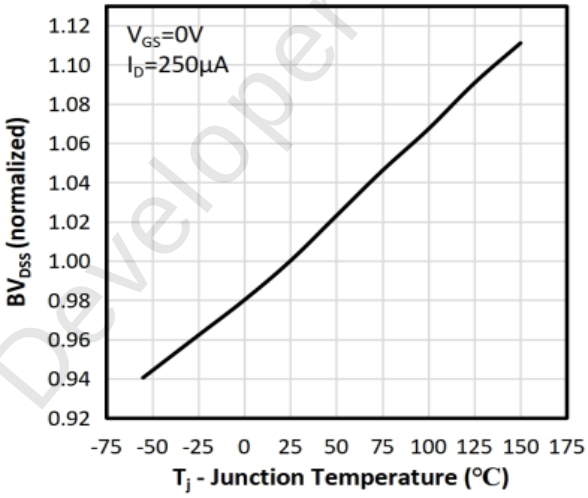
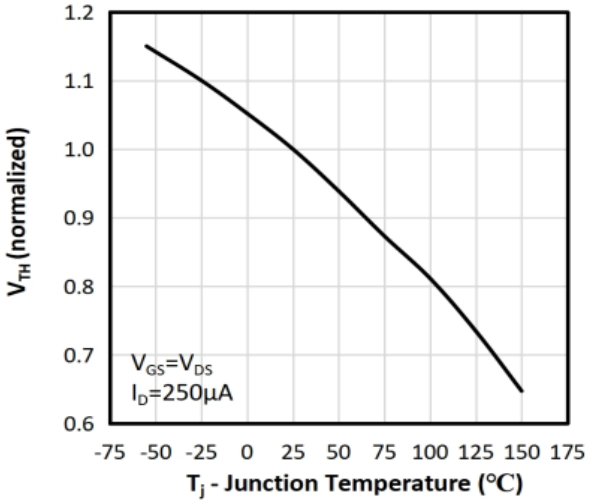


Fig 6: Threshold voltage vs. Temperature



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Fig 7: Body-Diode Characteristics

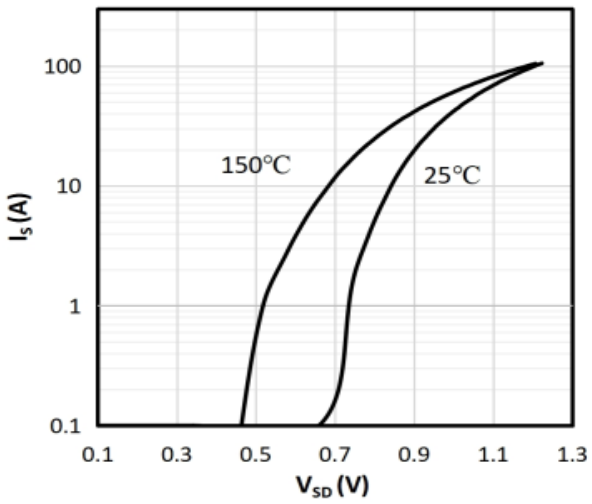


Fig 8: Capatitance Characteristics

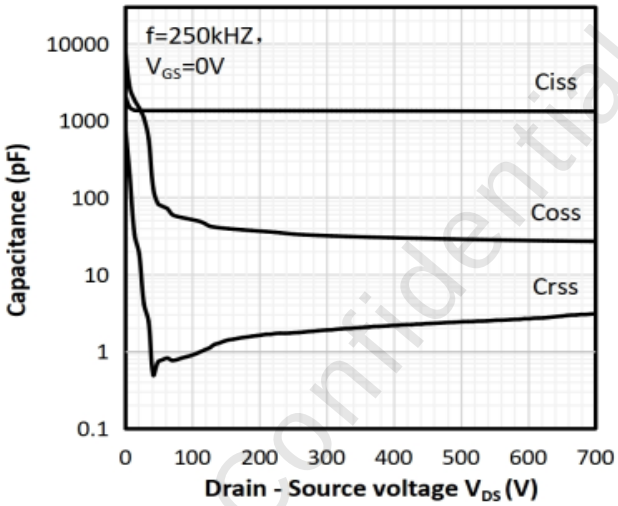


Fig 9: Gate charger Characteristics

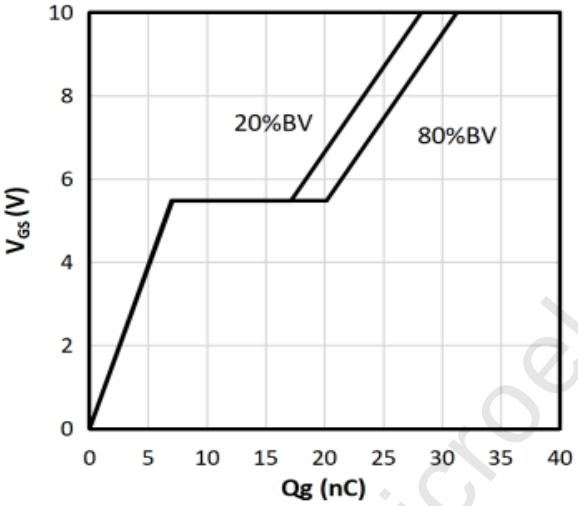


Fig 10: Drain Current Derating

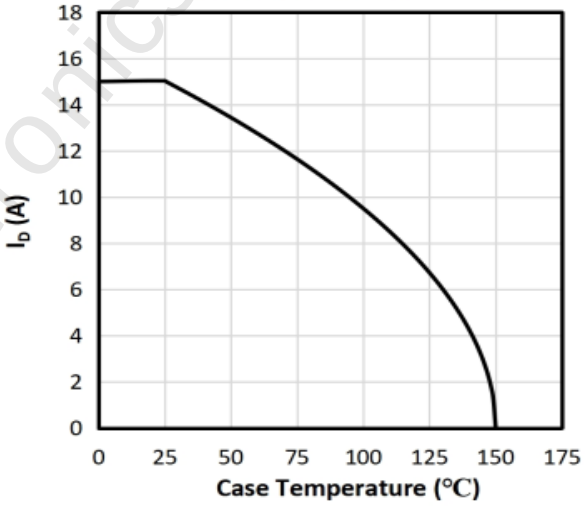


Fig 11: Power Dissipation vs.Temperature

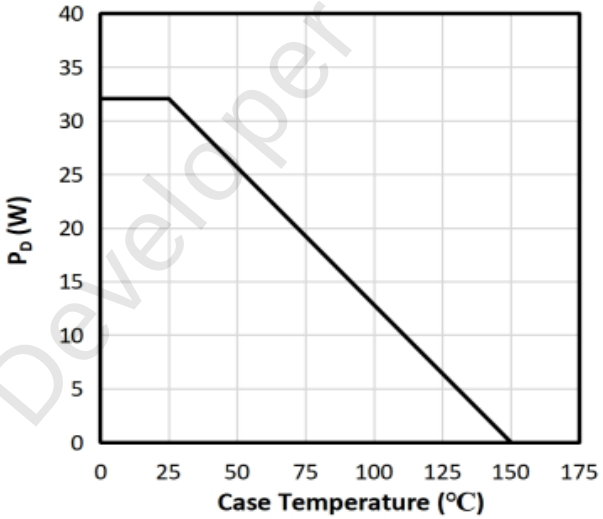
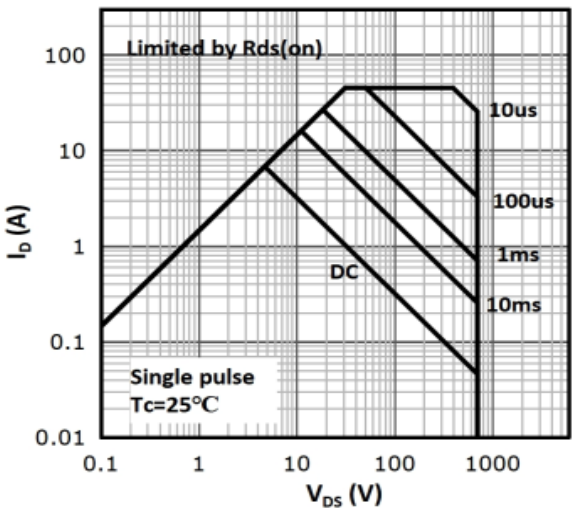
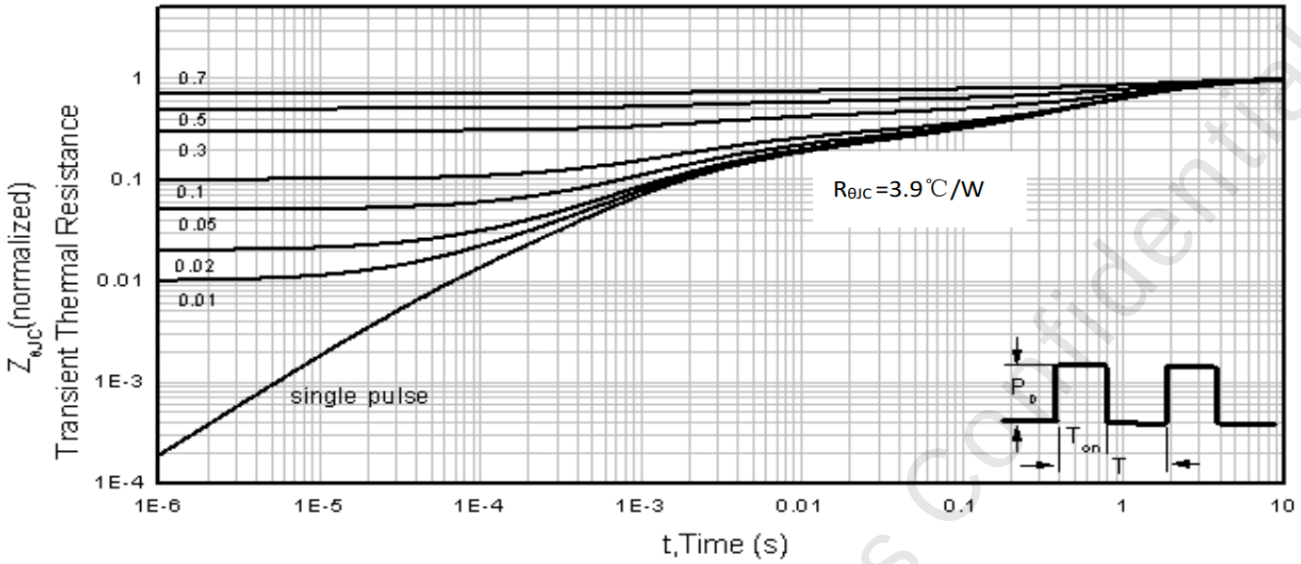


Fig 12: Safe Operating Area



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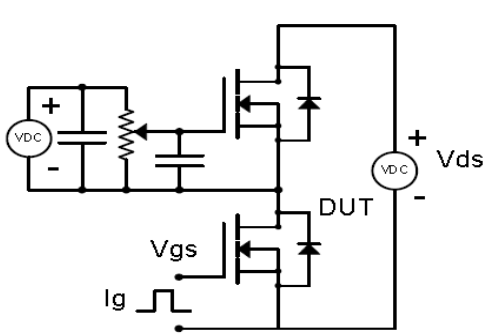
Fig 12: Max. Transient Thermal Impedance

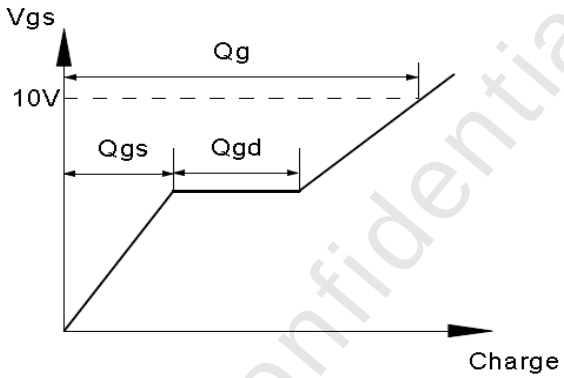


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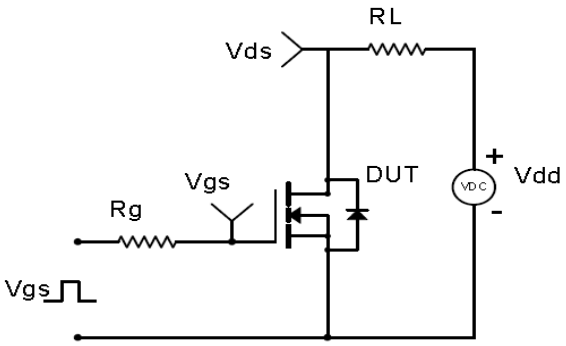
Test Circuit & Waveform

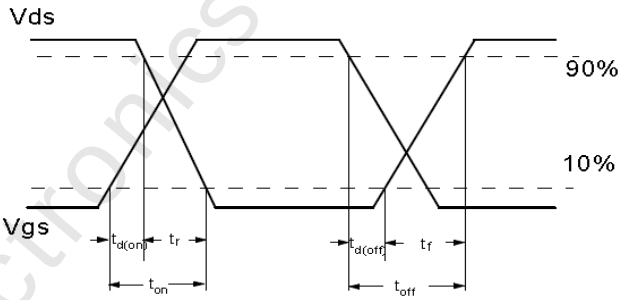
Gate Charge Test Circuit & Waveform



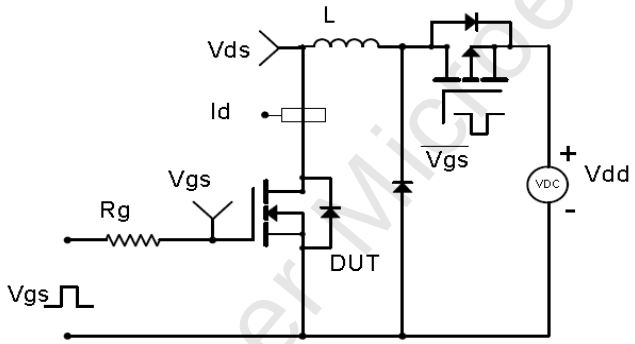


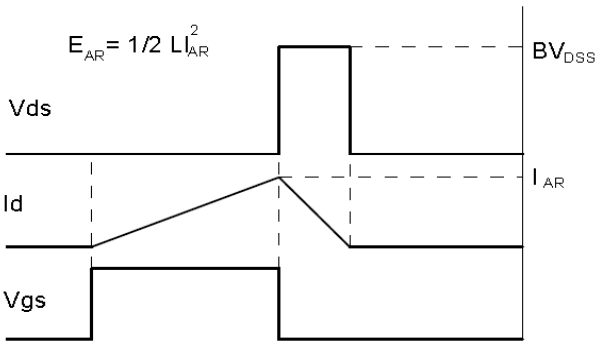
Resistive Switching Test Circuit & Waveforms



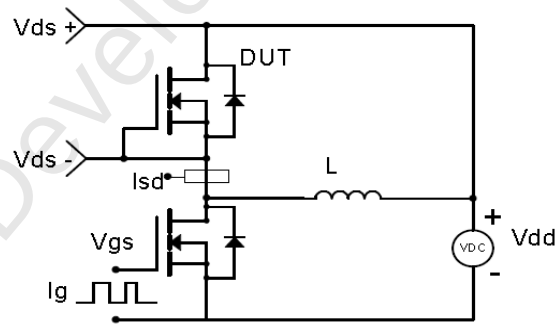


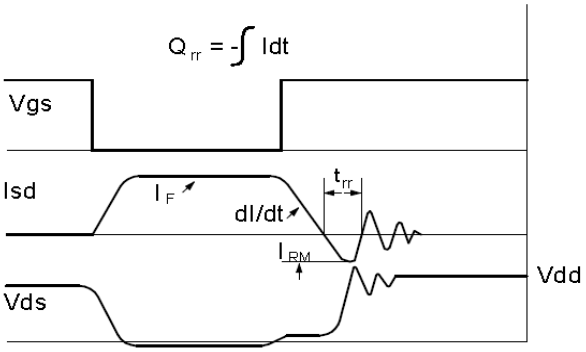
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





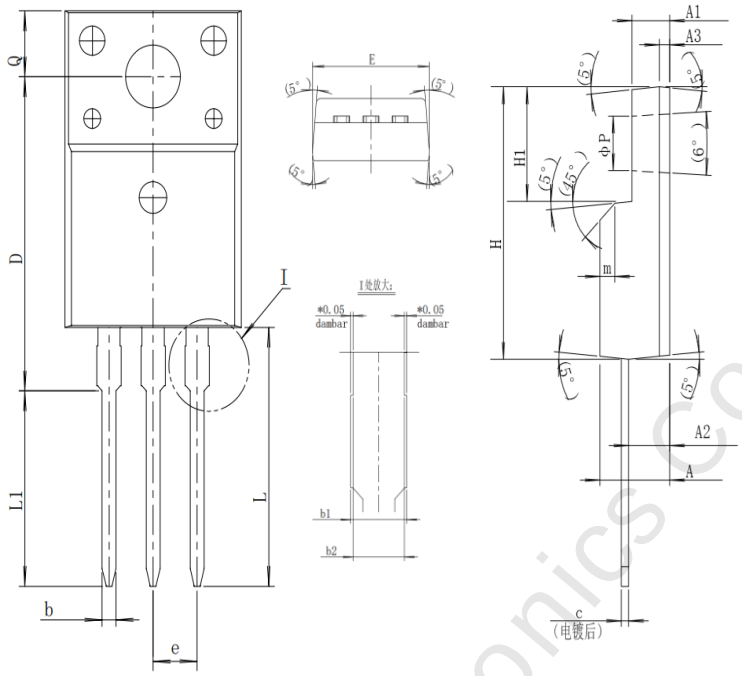
Diode Recovery Test Circuit & Waveforms





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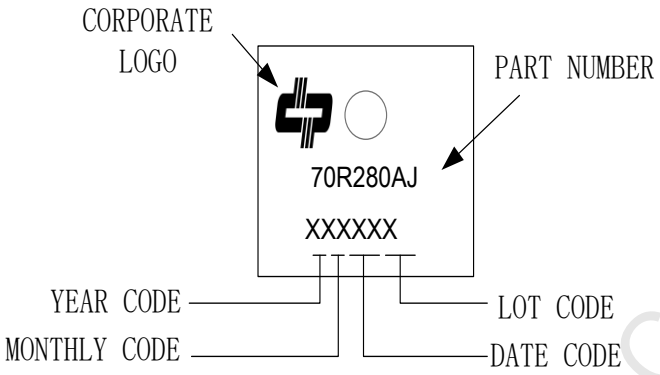
Package Outline: TO-220F



Symbol	Dimensions In Millimeters		
	Min.	NOM	Max.
A	4.60	4.70	4.80
A1	2.44	2.54	2.64
A2	2.65	2.75	2.85
A3		0.7 REF	
b	0.70	0.80	0.90
b1	1.28	1.38	1.47
b2	1.18	1.28	1.39
c	0.45	0.50	0.60
D	15.64	15.75	15.85
E	10.06	10.16	10.26
e		2.54 BSC	
H	15.77	15.87	15.97
H1	6.58	6.68	6.78
L	12.68	12.98	13.28
L1	9.60	9.80	10.00
Q	3.20	3.30	3.40
ΦP	3.08	3.18	3.28
m	0.50	1.00	1.50

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Part Marking Information



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Revision History

Revison	Major changes
1.0	Release for formal version

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