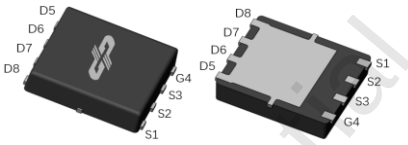
DP011N04FGLI

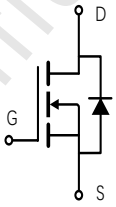
DPMOS N-MOSFET 40V, 0.92mΩ, 293A

Product Summary

Part #	V_{DS}	$R_{DS(on).typ}$ ($@V_{GS}$=10V)	$R_{DS(on).typ}$ ($@V_{GS}$=4.5V)	I_D
DP011N04FGLI	40V	0.92mΩ	1.25mΩ	293A

DFN 5x6





Features

- Uses advanced MOSFET-DPMOS2 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g x R_{DS(on)}$ product(FOM)
- Qualified according to JEDEC criteria(industrial grade)

Applications

- Motor control and drive
- Battery management
- UPS (Uninterrupible Power Supplies)

MSL-1

100% Avalanche Tested

100% Rg Tested

Package Marking and Ordering Information

Part #	Marking	Package	Packing
DP011N04FGLI	011N04FGL	DFN 5x6	Tape&Reel

Halogen-Free

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	40	V
Continuous drain current T_C = 25°C T_C = 100°C	I_D	 293 208	A
Pulsed drain current (T_C = 25°C, t_p limited by T_{jmax})	$I_{D\ pulse}$	1172	A
Avalanche energy, single pulse (L=0.3mH, Rg=25Ω)[1]	E_{AS}	421	mJ
Gate-Source voltage	V_{GS}	±20	V
Power dissipation (T_C = 25°C)	P_{tot}	160	W
Operating junction and storage temperature	T_j , T_{stg}	-55...+175	°C

[1].EAS is tested at starting Tj = 25℃, VGS = 10V.

Developer Microelectronics Confidential

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	0.9	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	52	

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	40	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{GS(th)}$	1.3	1.7	2.1	V	V_{DS}=V_{GS},I_D=250uA
Zero gate voltage drain current	I_{DSS}	- -	- 1	1 -	μA	V_{DS}=40V,V_{GS}=0V T_j=25°C T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	±100	nA	V_{GS}=±20V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.92 1.25	1.1 1.6	mΩ	V_{GS}=10V, I_D=40A V_{GS}=4.5V, I_D=32A
Gate resistance	R_g	-	2.5	5	Ω	V_{GS}=0V, V_{DS}=0V, f=1MHz
Transconductance[2]	g_{fs}	-	452	-	S	V_{DS}=5V,I_D=40A
Dynamic Characteristic[2]						
Input Capacitance	C_{iss}	-	5402	-	pF	V_{GS}=0V, V_{DS}=20V, f=1MHz
Output Capacitance	C_{oss}	-	1825	-		
Reverse Transfer Capacitance	C_{rss}	-	98	-		
Gate Total Charge	Q_g	-	86	-	nC	V_{GS}=10V, V_{DS}=20V, I_D=40A, f=1MHz
Gate-Source charge	Q_{gs}	-	22	-		
Gate-Drain charge	Q_{gd}	-	12	-		
Turn-on delay time	$t_{d(on)}$	-	15	-	ns	V_{GS}=10V, V_{DD}=20V, R_{G_ext}=2.7Ω
Rise time	t_r	-	46	-		
Turn-off delay time	$t_{d(off)}$	-	72	-		
Fall time	t_f	-	37	-		

Developer Microelectronics Confidential

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.75	1.3	V	V_{GS}=0V,I_{SD}=20A
Diode continuous forward current	I_s	-	-	293	A	TC = 25°C
Diode pluse current	$I_{s\ pluse}$	-	-	1172	A	TC = 25°C
Body Diode Reverse Recovery Time[2]	t_{rr}	-	48	-	ns	I_F=40A, dI/dt=100A/μs
Body Diode Reverse Recovery Charge[2]	Q_{rr}	-	42	-	nC	

[2]. Defined by design. Not subject to production test

Developer Microelectronics Confidential

Typical Performance Characteristics

Fig 1: Output Characteristics

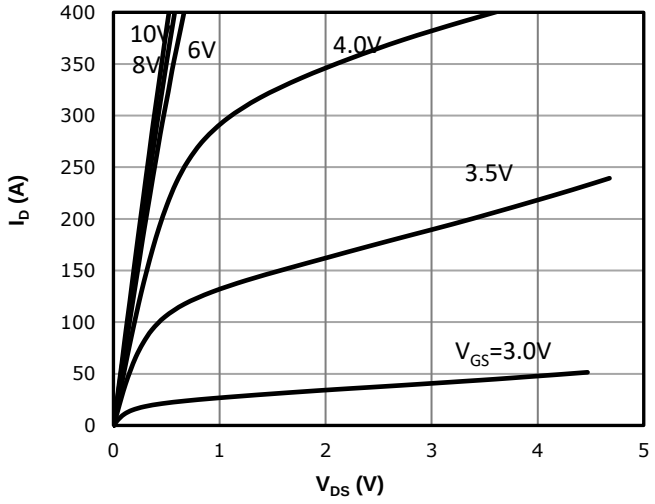


Fig 2: Transfer Characteristics

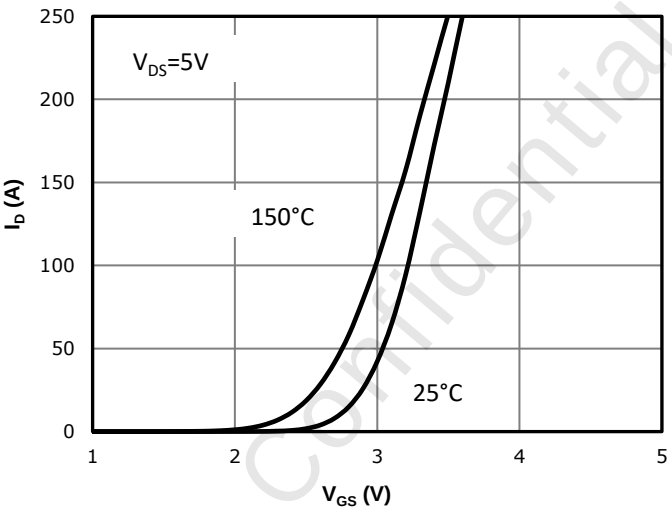


Fig 3: Rds(on) vs Drain Current and Gate Voltage

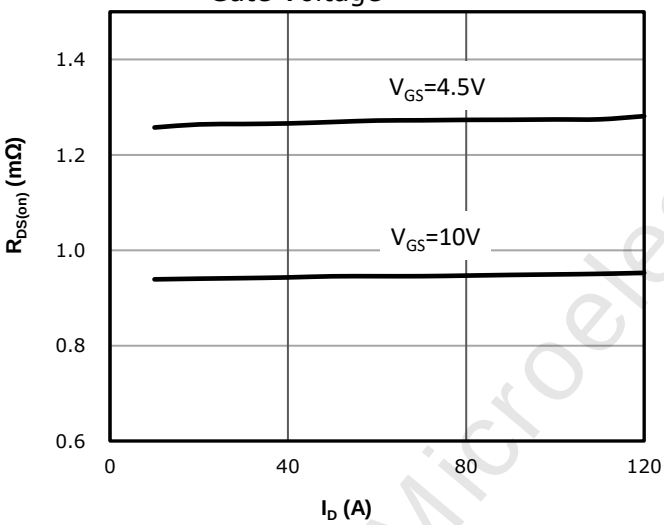


Fig 4: Rds(on) vs Gate Voltage

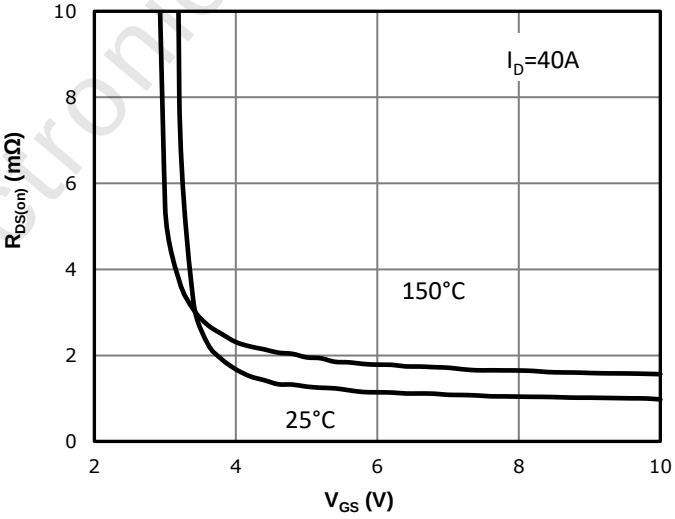


Fig 5: Rds(on) vs. Temperature

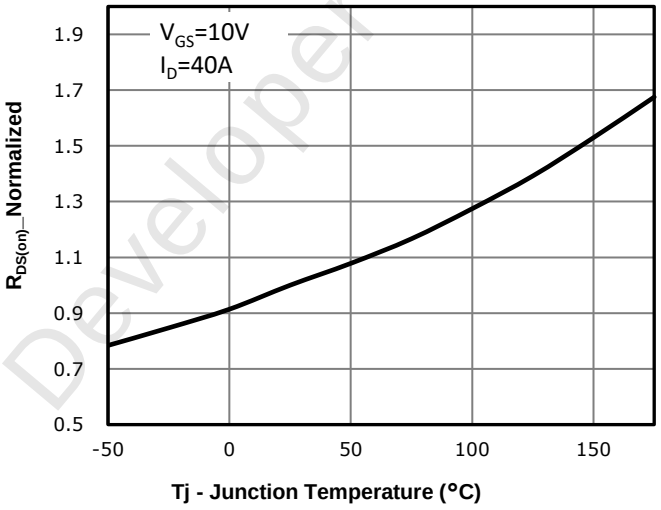
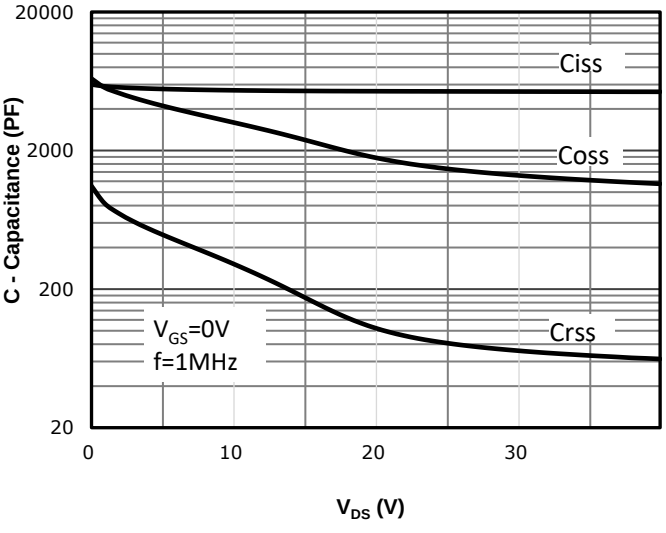


Fig 6: Capacitance Characteristics



Developer Microelectronics Confidential

Fig 7: Gate Charge Characteristics

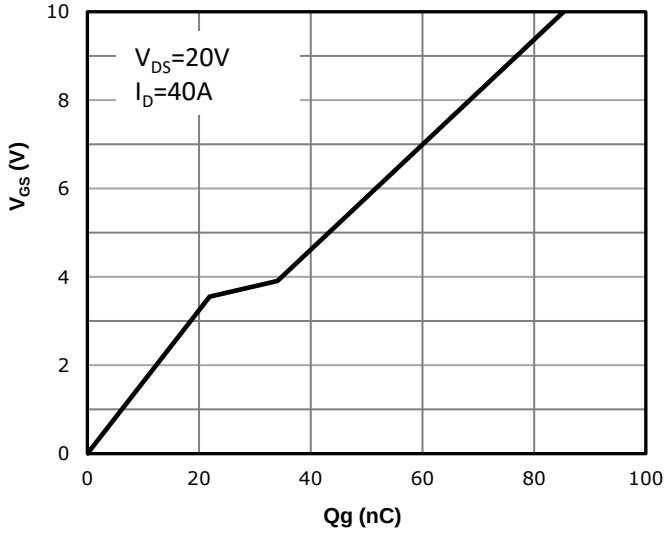


Fig 8: Body-diode Forward Characteristics

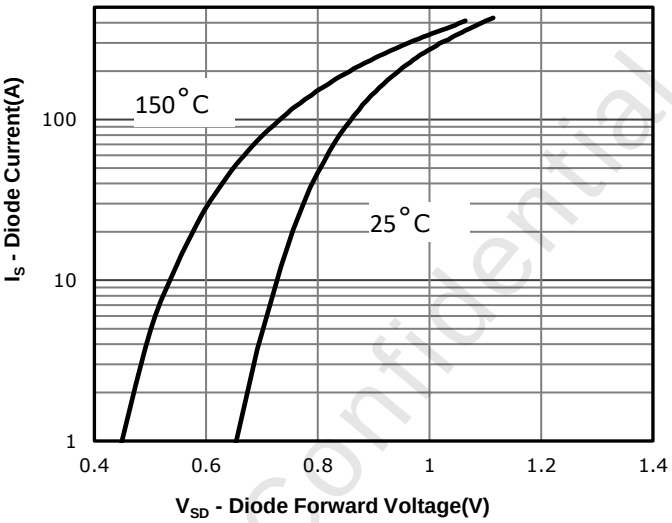


Fig 9: Power Dissipation

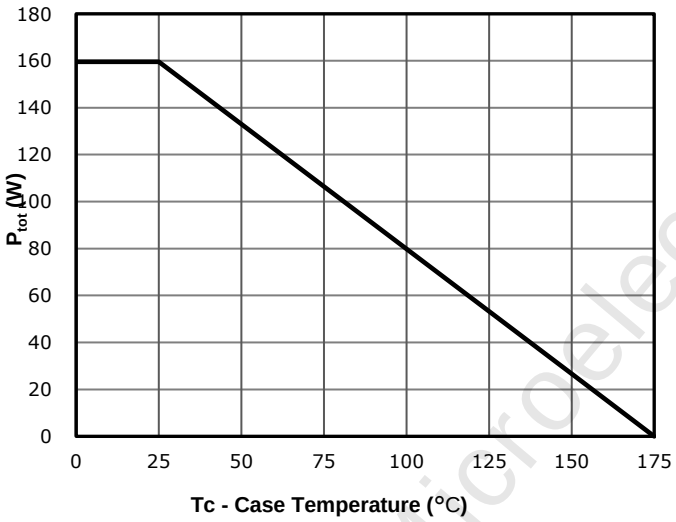


Fig 10: Drain Current Derating

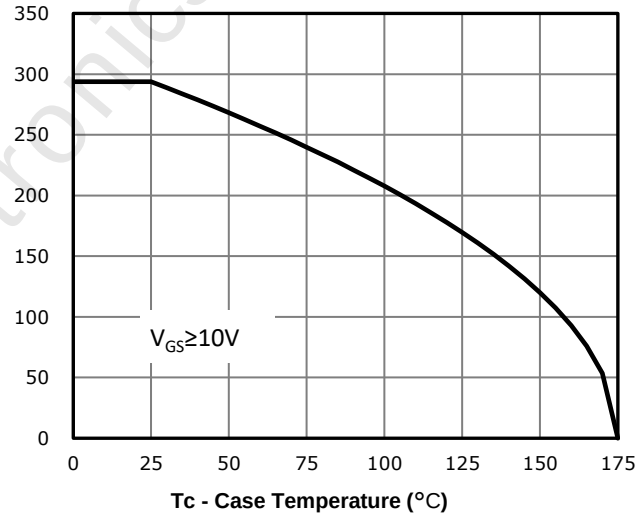
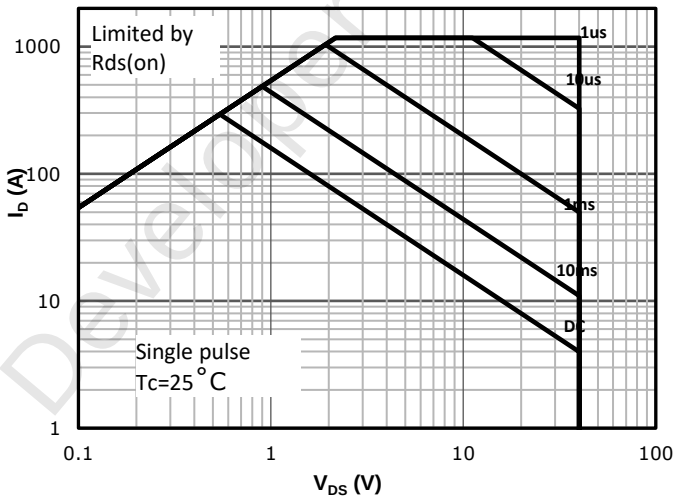
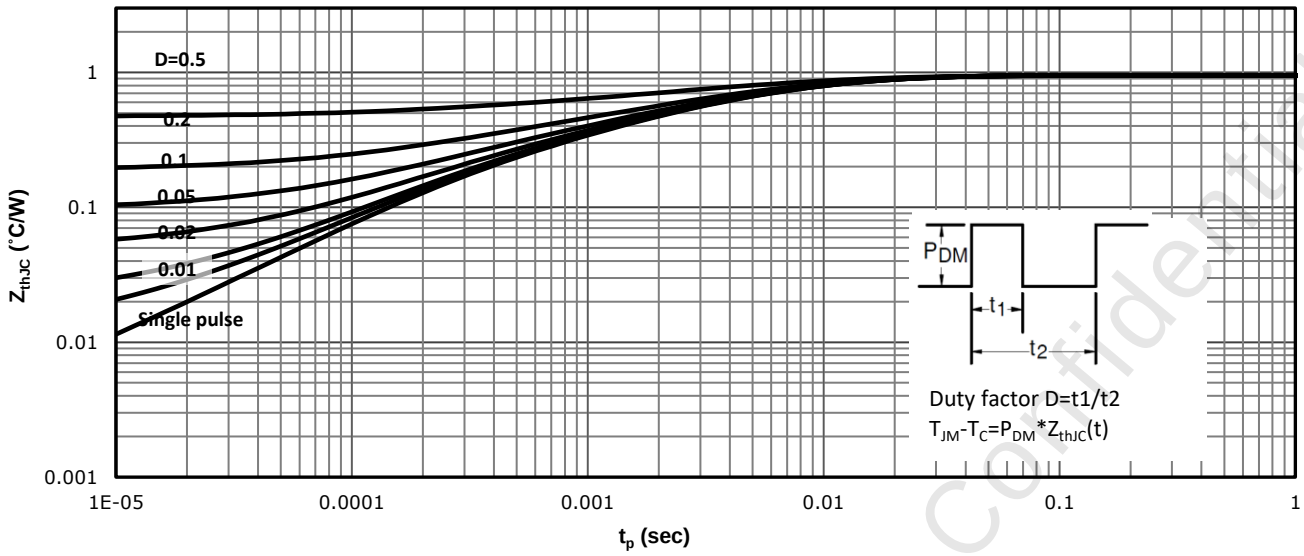


Fig 11: Safe Operating Area



Developer Microelectronics Confidential

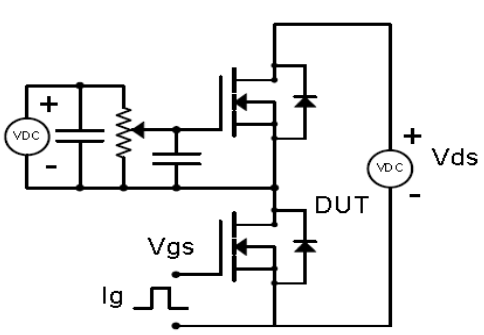
Fig 12: Max. Transient Thermal Impedance

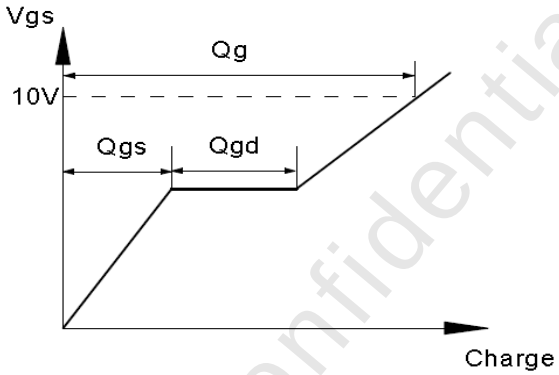


Developer Microelectronics Confidential

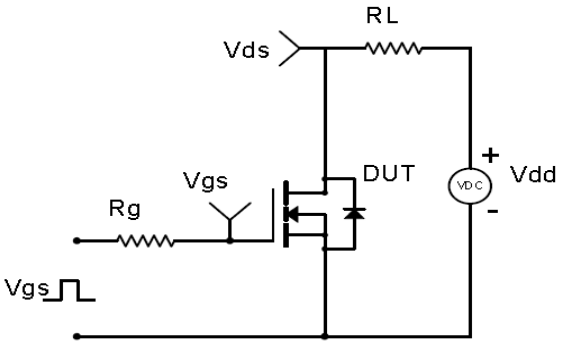
Test Circuit & Waveform

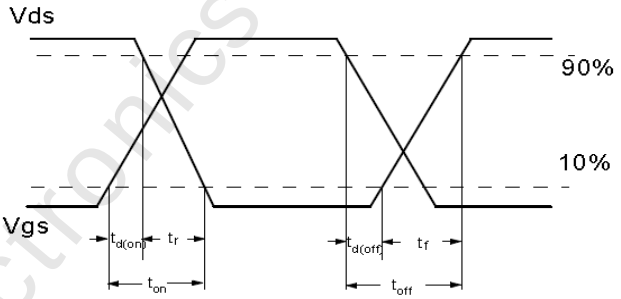
Gate Charge Test Circuit & Waveform



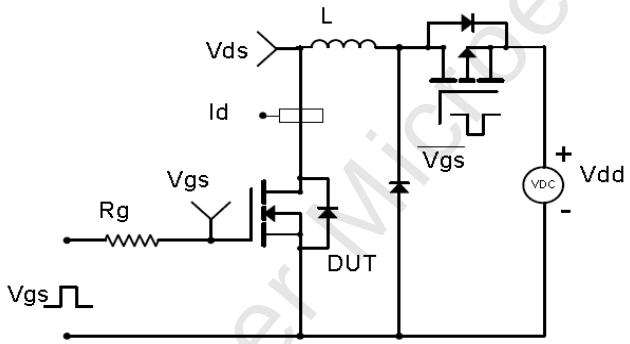


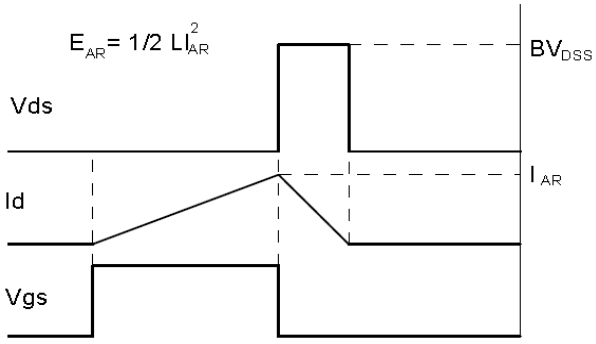
Resistive Switching Test Circuit & Waveforms



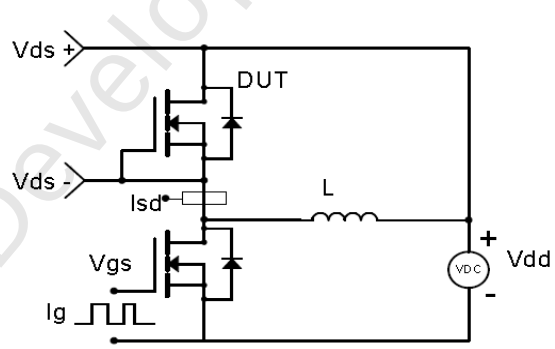


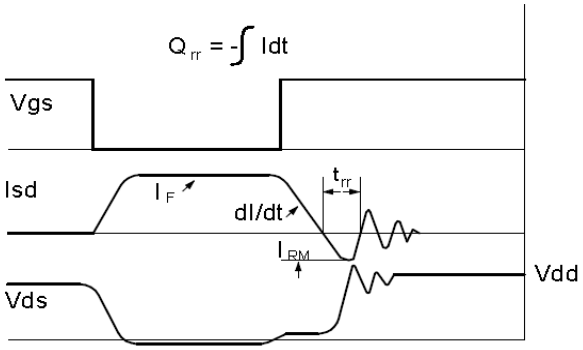
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





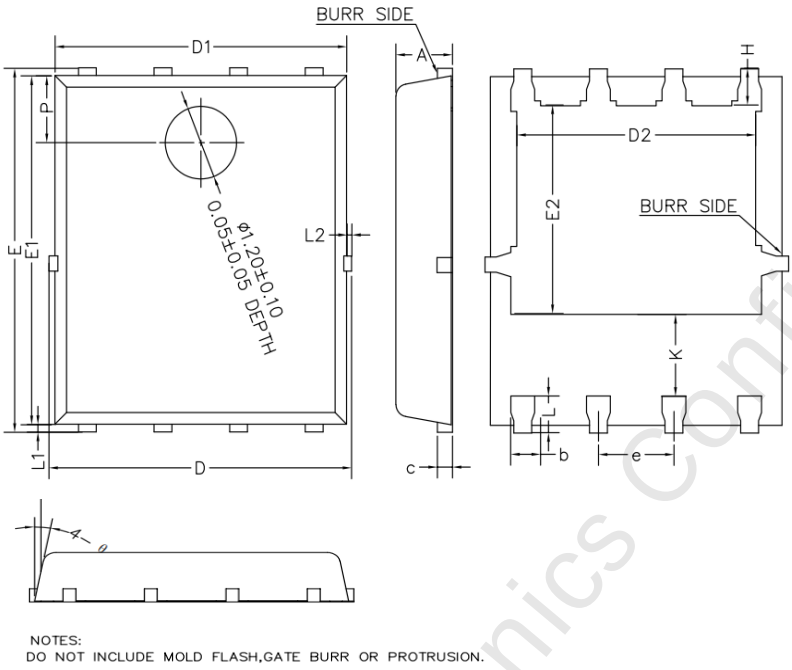
Diode Recovery Test Circuit & Waveforms





Developer Microelectronics Confidential

Package Outline: DFN5x6

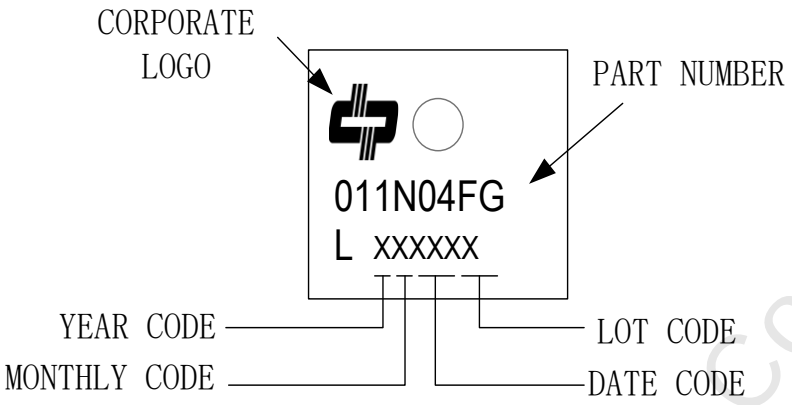


NOTES:
DO NOT INCLUDE MOLD FLASH,GATE BURR OR PROTRUSION.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.00	1.20	0.039	0.047
b	0.35	0.45	0.014	0.018
c	0.21	0.34	0.008	0.013
D	-	5.10	-	0.201
D1	4.90	5.00	0.193	0.197
D2	3.91	4.11	0.154	0.162
e	1.17	1.37	0.046	0.054
E	5.90	6.10	0.232	0.240
E1	5.70	5.80	0.224	0.228
E2	3.34	3.54	0.131	0.139
H	0.51	0.71	0.020	0.028
K	1.10	-	0.043	-
L	0.51	0.71	0.020	0.028
L1	0.06	0.20	0.002	0.008
L2	-	0.10	-	0.004
P	1.00	1.10	0.039	0.043
θ	8°	12°	-	-

Developer Microelectronics Confidential

Part Marking Information



Developer Microelectronics Confidential

Revision History

Revison	Major changes
1.5	Release for formal version

Developer Microelectronics Confidential

重要声明Important Notice

德普微尽力确保本产品规格书内容的准确和可靠，但是保留在没有通知的情况下，修改规格书内容的权利。客户在下订单前应联系德普微获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的本公司销售条款与条件。

德普微会不定期更新本文档内容，产品实际参数可能因型号或者其他事项不同有所差异，本文档不作为任何明示或暗示的担保或授权。

本产品规格书未包含任何针对德普微或第三方所有的知识产权的授权。针对本产品规格书所记载的信息，德普微不做任何明示或暗示的保证，包括但不限于对规格书内容的准确性、商业上的适销性，特定目的的适用性或者不侵犯德普微或任何第三人知识产权做任何明示或暗示保证，德普微也不就因本规格书本身及其使用有关的偶然或必然损失承担任何责任。

德普微对应用帮助或客户产品设计不承担任何义务。客户应对其使用本公司的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险，客户应提供充分的设计与操作安全验证。

针对本规格书所披露的内容，在未获得德普微的授权下，任何第三方不得使用、复制、转换，一经发现本公司必依法追究其法律责任，并赔偿由此对本公司造成的一切损失。

请注意在本资料记载的条件范围内使用产品，特别请注意绝对最大额定值、工作电压范围和电气特性等。 因在本资料记载的条件范围外使用产品而造成的故障和 (或) 事故等的损害，本公司对此概不承担任何责任。

本公司一直致力于提高产品的质量和可靠度，但所有的半导体产品都有一定的失效概率，这些失效概率可能会导致一些人身事故、火灾事故等。当设计产品时，请充分留意冗余设计并采用安全指标， 这样可以避免事故的发生。

使用本公司的IC生产产品时，如因其产品中对该IC的使用方法或产品的规格，或因进口国等原因，包含本IC产品在内的制品发生专利纠纷时，本公司概不承担相应责任。