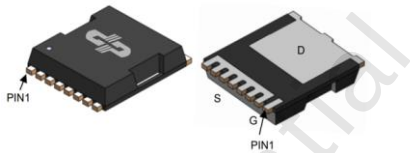
DPM075R060T8G2

N-Channel Silicon Carbide MOSFET

Product Summary

Part #	V_{DS}	$R_{DS(on)}$	I_D (T_{vj}=25℃)
DPM075R060T8G2	750V	51mΩ	38A

TOLL

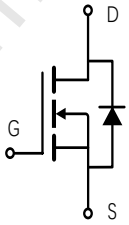


Features

- High Speed Switching with Low Capacitances
- High Blocking Voltage with Low $R_{DS(on)}$
- Easy to parallel
- RoHS Compliant

Applications

- General purpose drives
- Energy storage systems
- String inverter
- Uninterruptible power supplies



Package Marking and Ordering Information

Part #	Marking	Package	Packing
DPM075R060T8G2	M075R060T8	TOLL	Tape/Reel

Halogen-Free

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	750	V
Continuous drain current T_C = 25°C T_C = 100°C	I_D	 38 27	A
Pulsed drain current (T_C = 25°C, t_p limited by T_{jmax})	$I_{D\ pulse}$	95	A
Avalanche energy, single pulse (L=0.5mH, Rg=25)[1]	E_{AS}	135	mJ
Gate-source voltage, max. transient voltage	V_{GSmax}	-10/+22	V
Gate-source voltage, max. static voltage	V_{GSop}	0/+15	V
Power dissipation (T_C = 25°C) Power dissipation (T_C = 100°C)	P_{tot}	120 60	W
Operating junction temperature	T_j	-40...+175	°C
Storage temperature	T_{stg}	-40...+175	°C

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – mounting base	R_{thMB}	1.3	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	50	

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Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	750	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{GS(th)}$	2.5	3.3 2.3		V	V_{DS}=V_{GS},I_D=3.5mA T_j=25°C T_j=175°C
Zero gate voltage drain current	I_{DSS}	-	0.01	1	μA	V_{DS}=750V,V_{GS}=0V T_j=25°C
Gate-source leakage current	I_{GSS}	-	-	250	nA	V_{GS}=22V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	67 87	87	mΩ	V_{GS}=15V, I_D=12.5A T_j=25°C T_j=175°C
		-	51 62	64	mΩ	V_{GS}=18V, I_D=12.5A T_j=25°C T_j=175°C
Gate resistance	R_g	-	4.2	-	Ω	V_{GS}=0V, V_{AC}=25mV, f=1MHz
Dynamic Characteristic[2]						
Input Capacitance	C_{iss}	-	1021	-	pF	V_{GS}=0V, V_{DS}=500V, f=1MHz
Output Capacitance	C_{oss}	-	93	-		
Reverse Transfer Capacitance	C_{rss}	-	6	-		
Gate Total Charge	Q_g	-	49	-	nC	V_{GS}=0/15V, V_{DS}=500V, I_D=16.5A, f=1MHz
Gate-Source charge	Q_{gs}	-	14	-		
Gate-Drain charge	Q_{gd}	-	8	-		
Turn-on delay time	$t_{d(on)}$	-	7	-	ns	V_{GS}=-5/18V, V_{DD}=500V, R_{G_ext}=10Ω
Rise time	t_r	-	14	-		
Turn-off delay time	$t_{d(off)}$	-	24	-		
Fall time	t_f	-	12	-		

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Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	4 3.5	6	V	V_{GS}=-5V,I_{SD}=12.5A T_j=25°C T_j=175°C
Diode continuous forward current	I_s		35 20	- -	A	V_{GS}=-4V T_C = 25°C T_C = 100°C
Diode Peak reverse recovery Current	I_{rrm}	-	39	-	A	VGS=-5V,V_R=500V I_{SD}=12.5A, dI/dt=4000A/µs
Body Diode Reverse Recovery Time[2]	t_{rr}	-	14	-	ns	
Body Diode Reverse Recovery Charge[2]	Q_{rr}	-	195	-	nC	

[2]. Defined by design. Not subject to production test

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Typical Performance Characteristics

Fig 1: Output Characteristics
Tj=-55 ℃

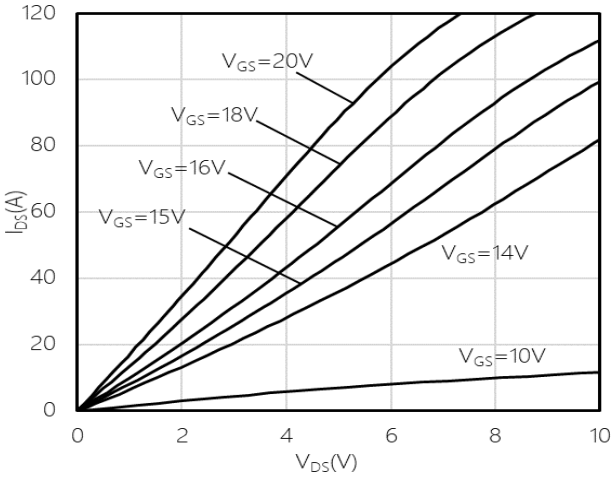


Fig 2: Output Characteristics
Tj=25 ℃

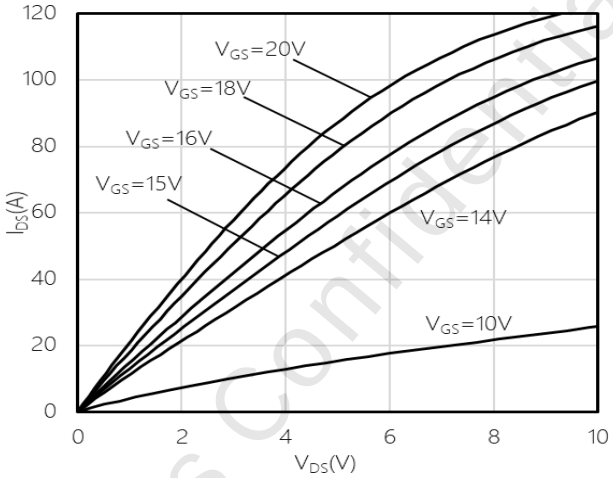


Fig 3: Output Characteristics
Tj=175 ℃

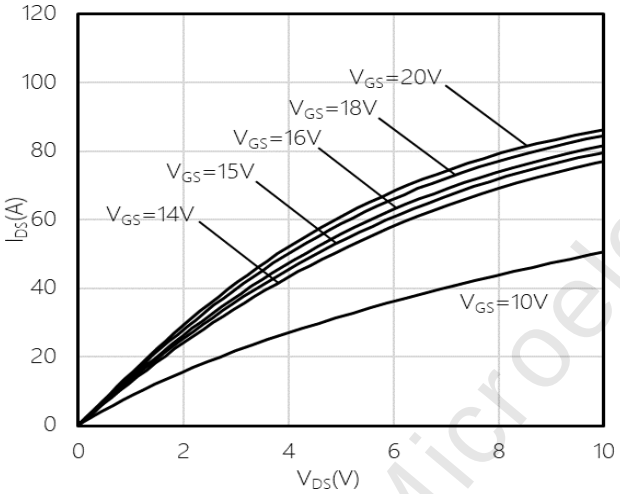


Fig 4: Typical on-state resistance as a function of drain current

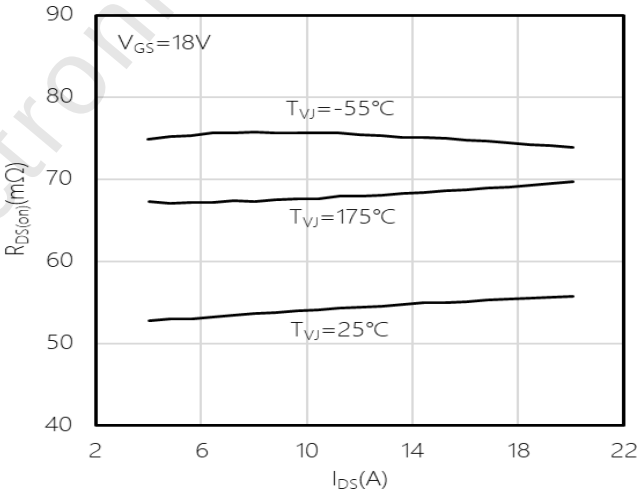


Fig 5: Typical on-state resistance as a function of temperature

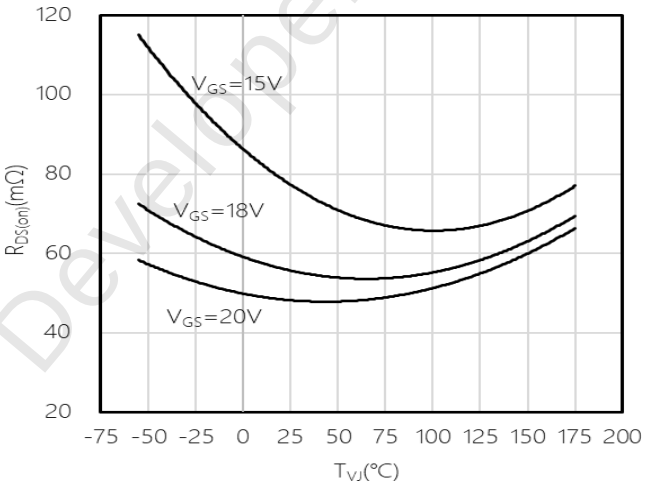
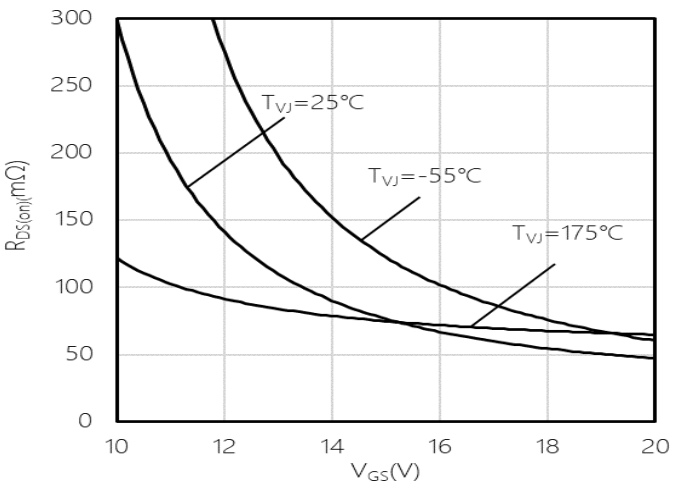


Fig 6: Typical on-state resistance as a function of VGS



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Fig 7: Typical transfer characteristic

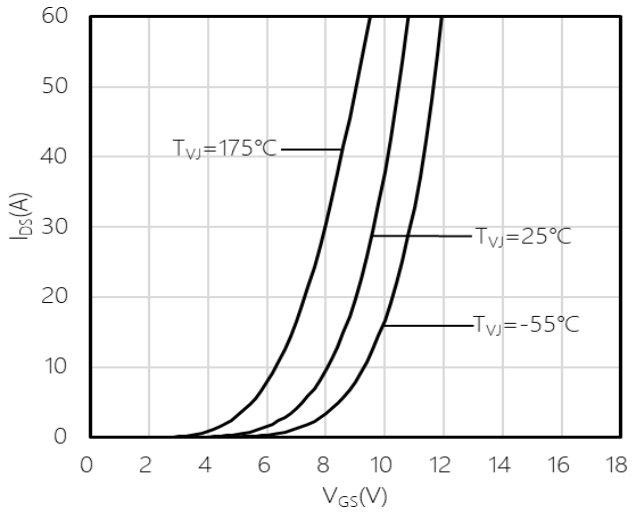


Fig 8: Typical Vth as a function of junction temperature

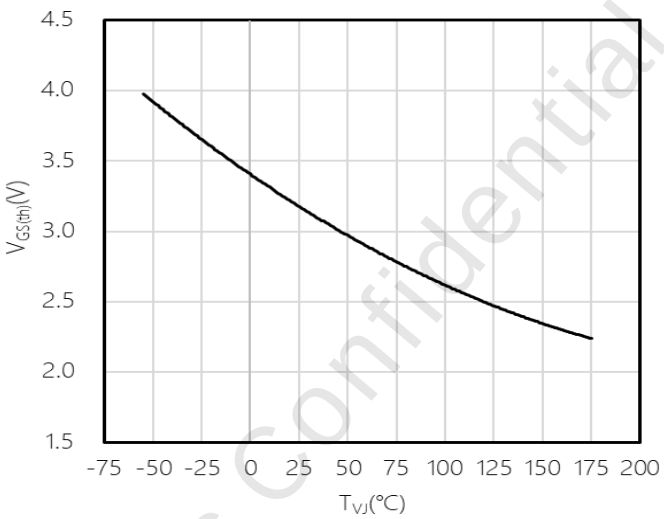


Fig 9: Typical reverse drain current as function of reverse drain voltage ;Tj=-55 ℃

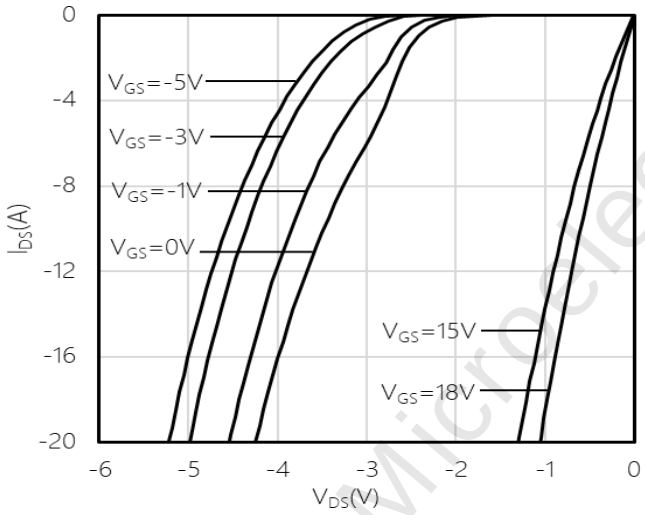


Fig 10: Typical reverse drain current as function of reverse drain voltage ;Tj=25 ℃

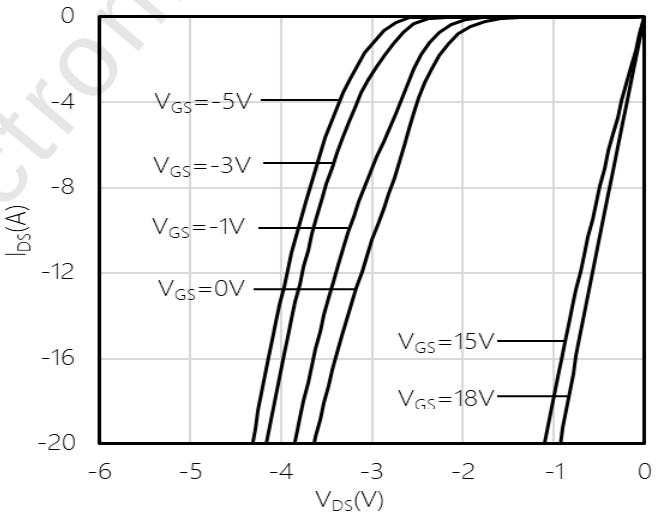


Fig 11: Typical reverse drain current as function of reverse drain voltage ;Tj=175℃

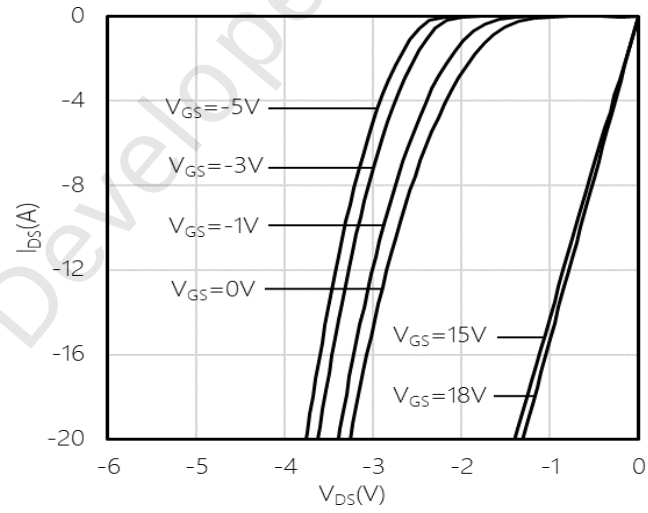
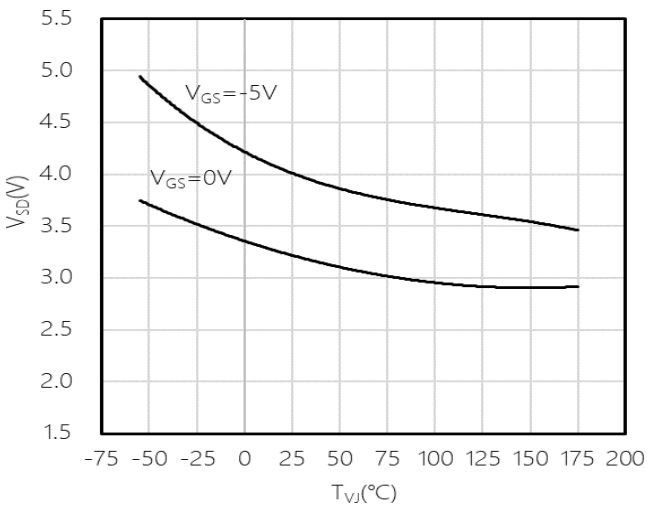


Fig 12: Typical reverse drain voltage as function of junction temperature



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Fig 13: Typical gate charge

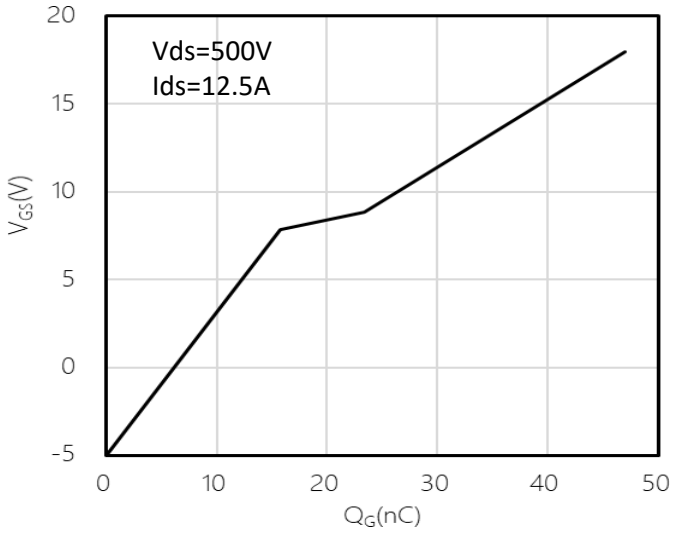


Fig 14: Typical capacitance as a function of drain-source voltage

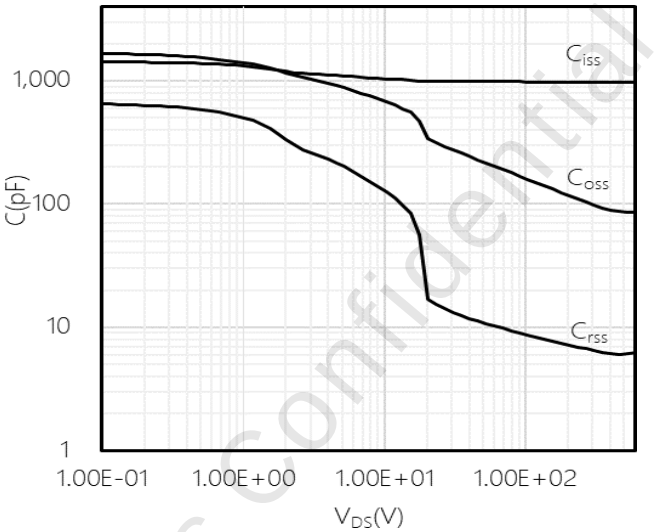


Fig 15: Drain Current Derating

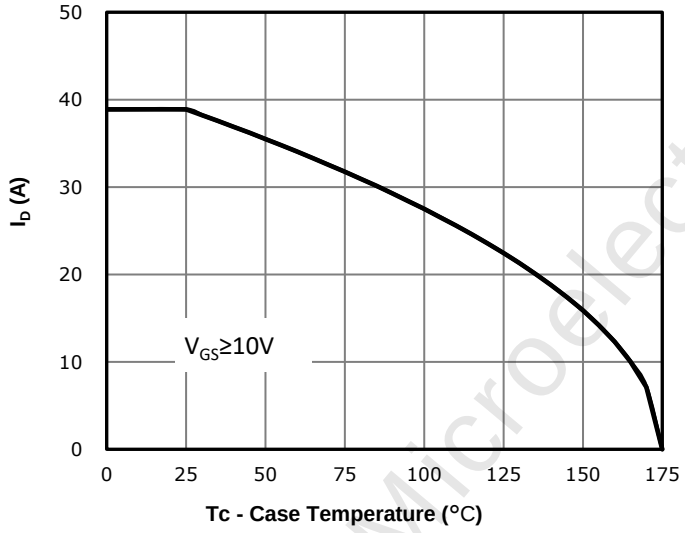


Fig 16: Safe Operating Area

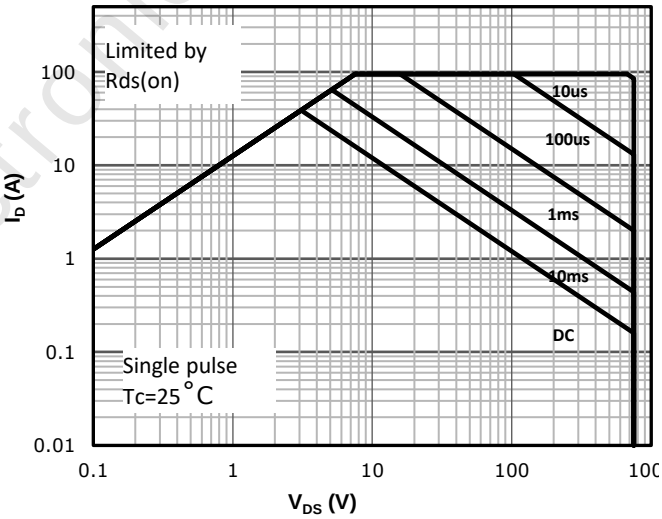
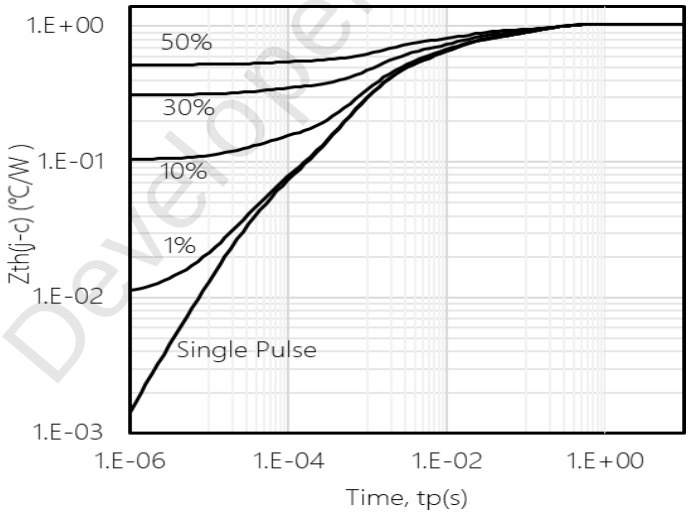


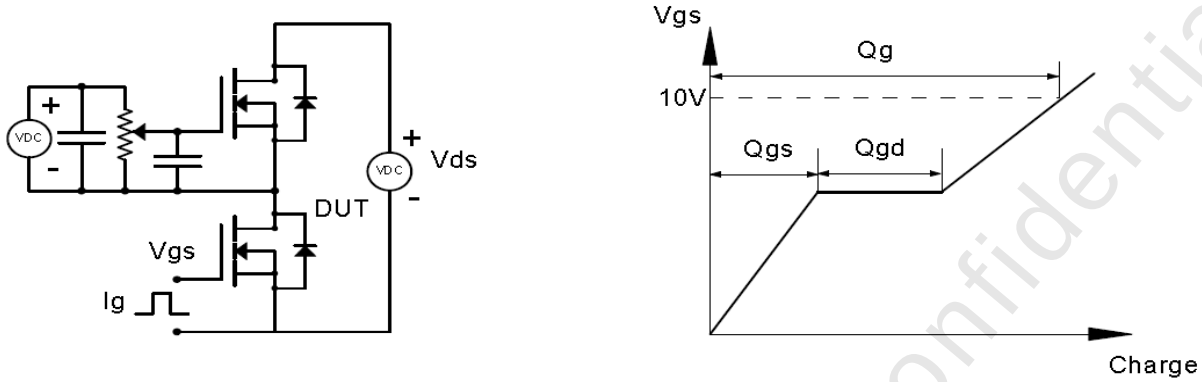
Fig 17: Transient thermal resistance (MOSFET)



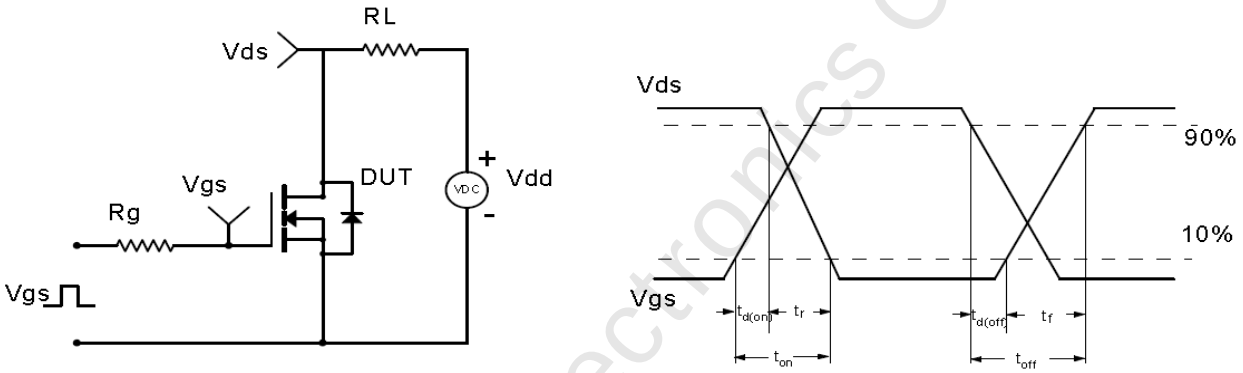
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Test Circuit & Waveform

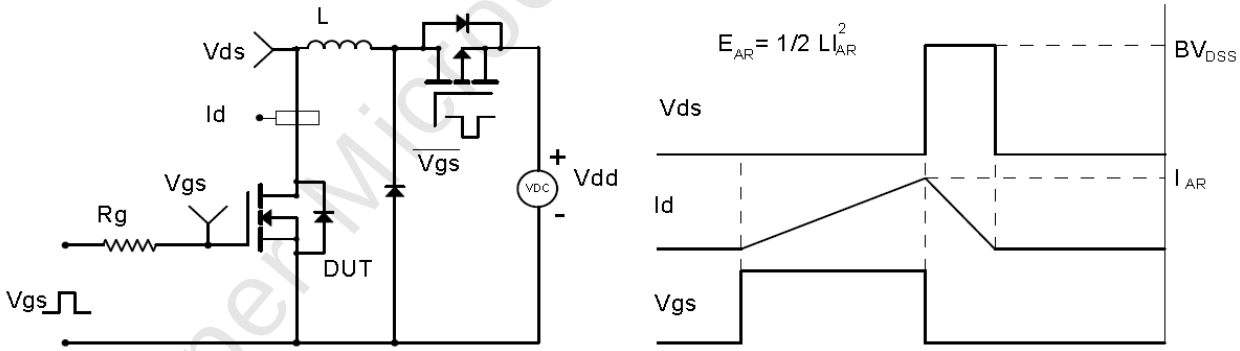
Gate Charge Test Circuit & Waveform



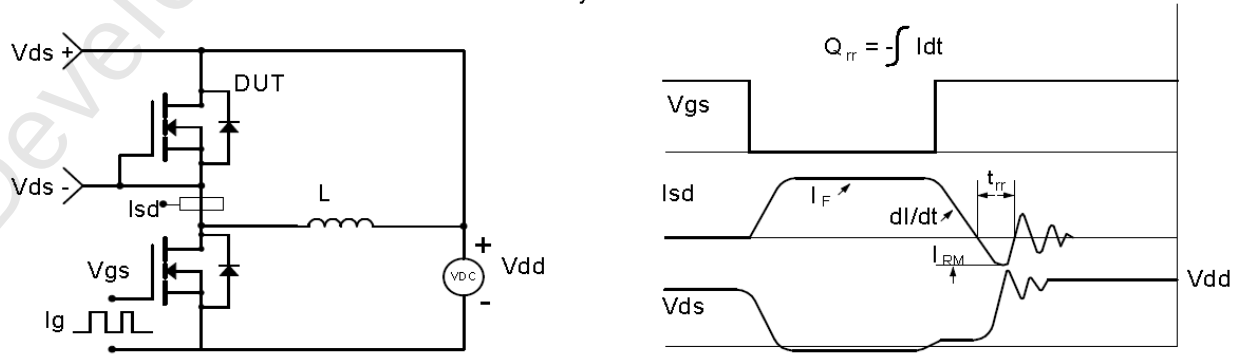
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

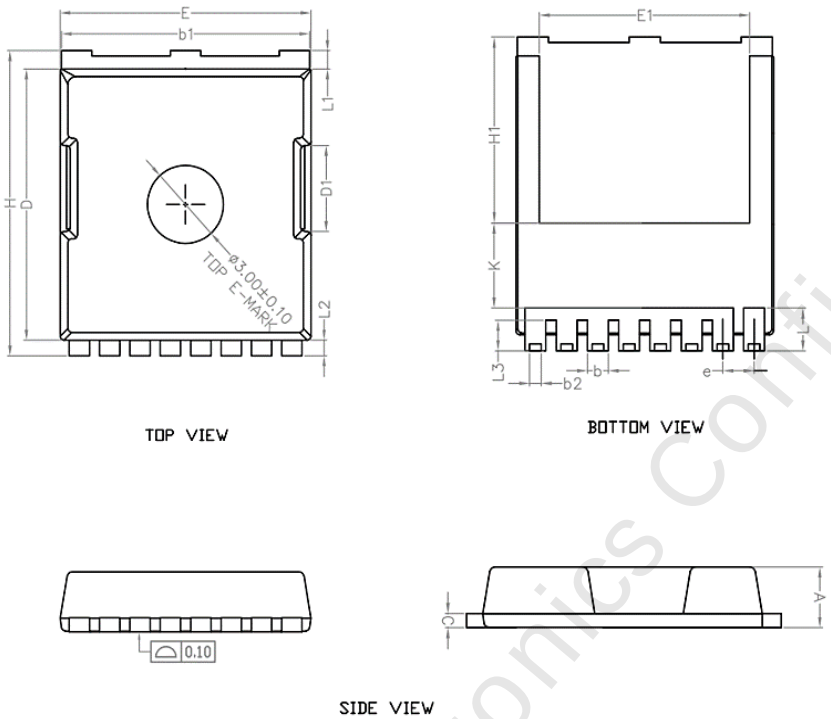


Diode Recovery Test Circuit & Waveforms



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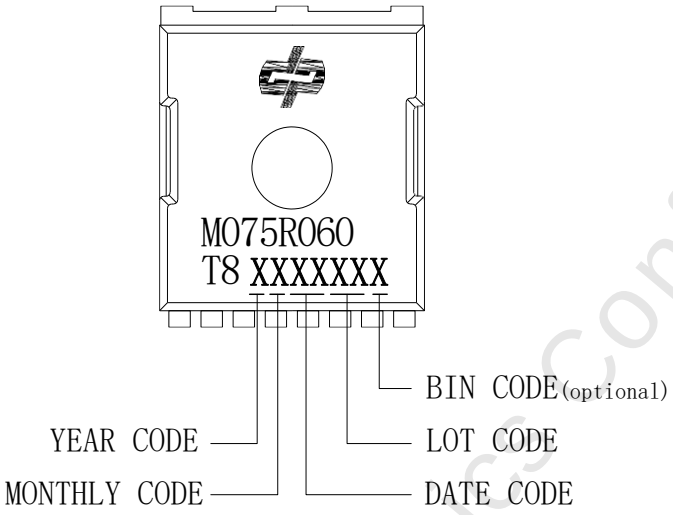
Package Outline: TOLL



Symbol	Common Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.20	2.40	0.09	0.09
b	0.70	0.90	0.03	0.04
b1	9.70	9.90	0.38	0.39
b2	0.40	0.50	0.02	0.02
c	0.40	0.60	0.02	0.02
D	10.28	10.58	0.40	0.42
D1	3.15	3.45	0.12	0.14
E	9.70	10.10	0.38	0.40
E1	7.90	8.30	0.31	0.33
e	1.10	1.30	0.04	0.05
H	11.48	11.88	0.45	0.47
H1	6.75	7.15	0.27	0.28
K	3.03	3.33	0.12	0.13
L	1.50	1.70	0.06	0.07
L1	0.55	0.85	0.02	0.03
L2	0.45	0.75	0.02	0.03
L3	1.00	1.30	0.04	0.05

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Part Marking Information



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Revision History

Revison	Major changes
1.0	Release for formal version

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