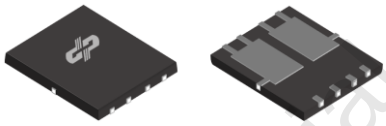
DP065N04FGNB

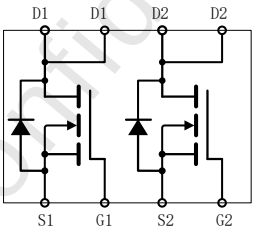
DPMOS N-MOSFET 40V, 5.2mΩ, 55A

Product Summary

Part #	V_{DS}	$R_{DS(on).typ}$	I_D
DP065N04FGNB	40V	5.2mΩ	55A

DFN5x6-8





Features

- Uses advanced MOSFET-DPMOS2 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent Q_gx$R_{DS(on)}$ product(FOM)
- Qualified according to JEDEC criteria

Applications

- Motor control and drive
- Battery management
- UPS (Uninterrupible Power Supplies)

MSL-1

100% Avalanche Tested

Package Marking and Ordering Information

Part #	Marking	Package	Packing
DP065N04FGNB	065N04FGNB	DFN5x6-8	Tape&Reel

Halogen-Free

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	40	V
Continuous drain current T_C = 25°C T_C = 100°C	I_D	 55 35	A
Pulsed drain current (T_C = 25°C, t_p limited by T_{jmax})	$I_{D\ pulse}$	220	A
Avalanche energy, single pulse (L=0.3mH, Rg=25Ω)[1]	E_{AS}	100	mJ
Gate-Source voltage	V_{GS}	±20	V
Power dissipation (T_C = 25°C)	P_{tot}	31	W
Operating junction and storage temperature	T_j , T_{stg}	-55...+150	°C

[1].EAS is tested at starting Tj = 25℃, VGS = 10V.

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	4	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	75	

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	40	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{GS(th)}$	2.4	3	3.6	V	V_{DS}=V_{GS},I_D=250uA
Zero gate voltage drain current	I_{DSS}	- -	- -	1 100	μA	V_{DS}=40V,V_{GS}=0V T_j=25°C T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	±100	nA	V_{GS}=±20V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	5.2 5.4	6.5 7.0	mΩ	V_{GS}=10V, I_D=12A V_{GS}=8V, I_D=10A
Gate resistance	R_g	-	2	5	Ω	V_{GS}=0V, V_{DS}=0V, f=1MHz
Transconductance[2]	g_{fs}	-	105	-	S	V_{DS}=5V,I_D=20A
Dynamic Characteristic[2]						
Input Capacitance	C_{iss}	-	1577	-	pF	V_{GS}=0V, V_{DS}=20V, f=1MHz
Output Capacitance	C_{oss}	-	513	-		
Reverse Transfer Capacitance	C_{rss}	-	32	-		
Gate Total Charge	Q_g	-	27	-	nC	V_{GS}=10V, V_{DS}=20V, I_D=20A, f=1MHz
Gate-Source charge	Q_{gs}	-	10	-		
Gate-Drain charge	Q_{gd}	-	3.6	-		
Turn-on delay time	$t_{d(on)}$	-	4.2	-	ns	V_{GS}=10V, V_{DD}=20V, R_{G_ext}=2.7Ω
Rise time	t_r	-	29	-		
Turn-off delay time	$t_{d(off)}$	-	19	-		
Fall time	t_f	-	13	-		

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.8	1.3	V	V_{GS}=0V,I_{SD}=15A
Diode continuous forward current	I_s	-	-	55	A	TC = 25°C
Diode pluse current	$I_{s\ pluse}$	-	-	220	A	TC = 25°C
Body Diode Reverse Recovery Time[2]	t_{rr}	-	20	-	ns	I_F=20A, dI/dt=50A/μs
Body Diode Reverse Recovery Charge[2]	Q_{rr}	-	4	-	nC	

[2]. Defined by design. Not subject to production test

Typical Performance Characteristics

Fig 1: Output Characteristics

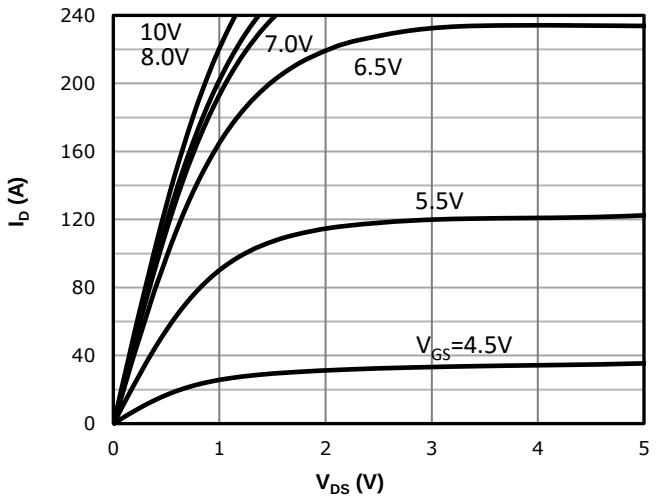


Fig 2: Transfer Characteristics

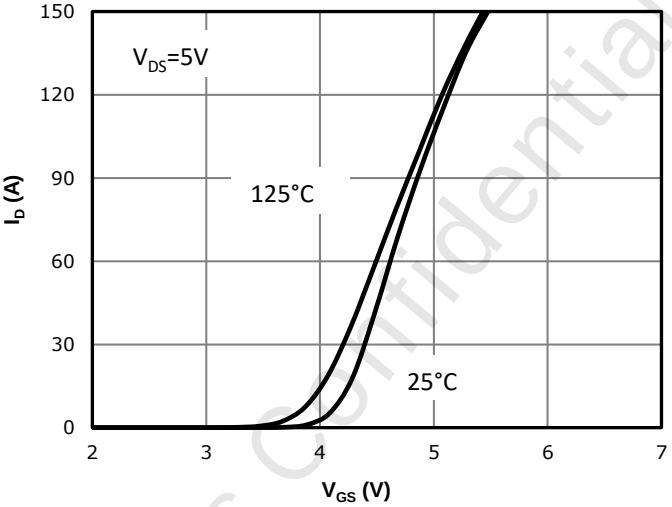


Fig 3: Rds(on) vs Drain Current and Gate Voltage

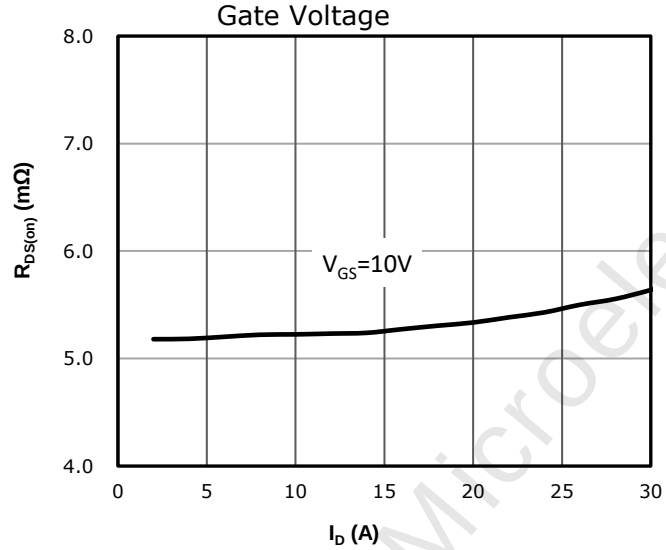


Fig 4: Rds(on) vs Gate Voltage

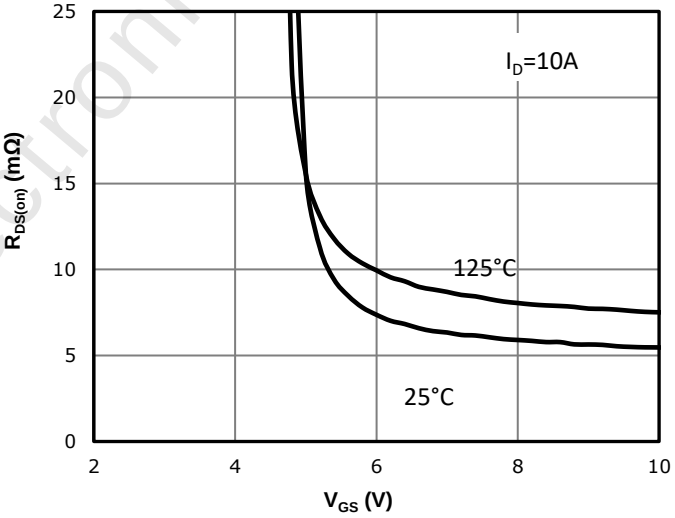


Fig 5: Rds(on) vs. Temperature

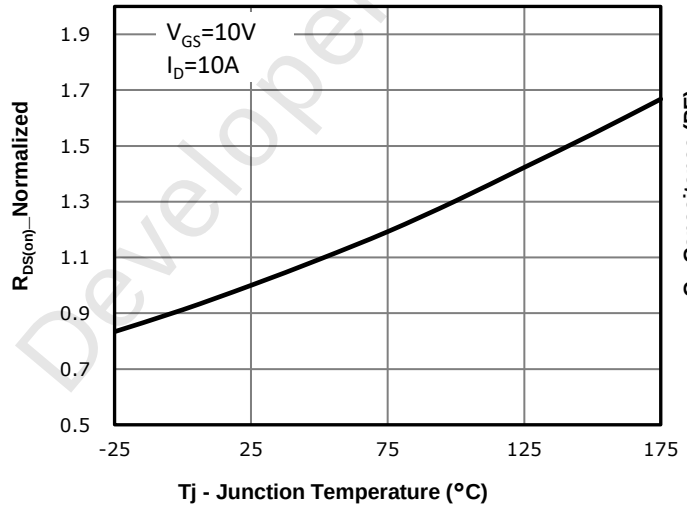


Fig 6: Capacitance Characteristics

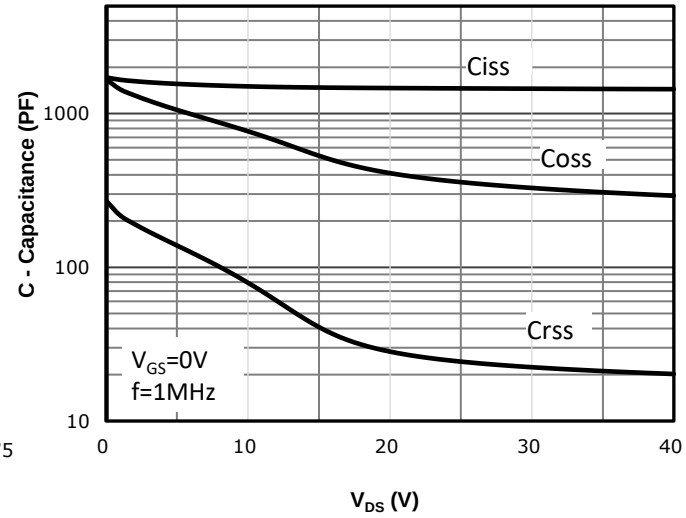


Fig 7: Gate Charge Characteristics

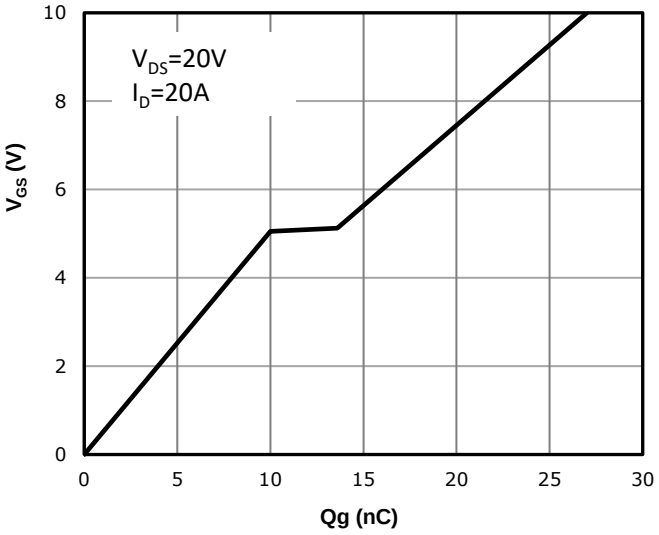


Fig 8: Body-diode Forward Characteristics

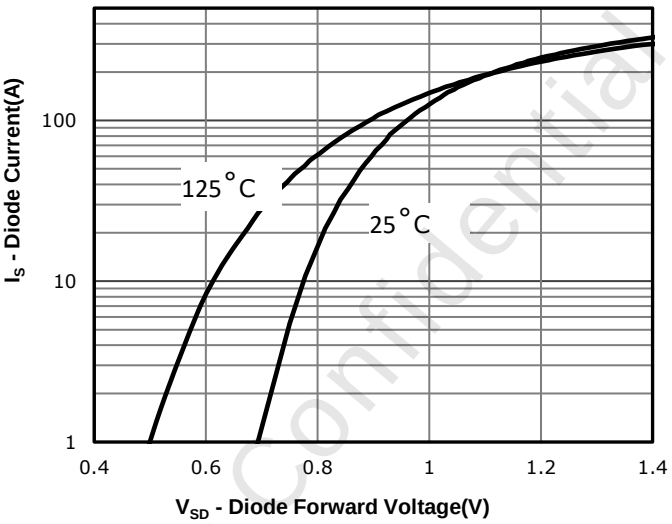


Fig 9: Power Dissipation

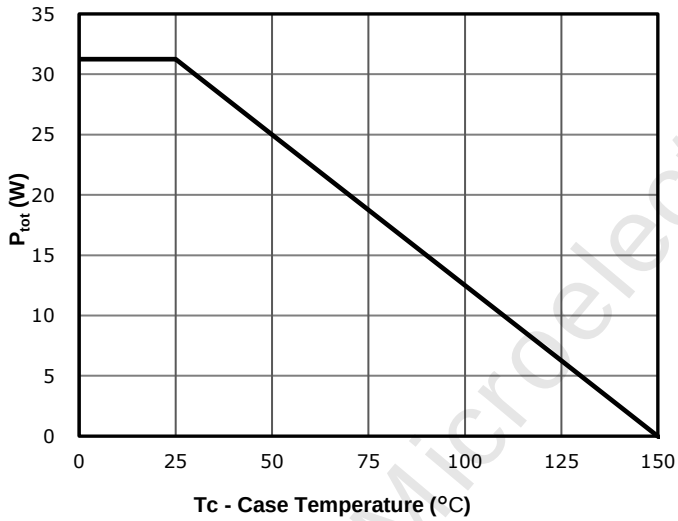


Fig 10: Drain Current Derating

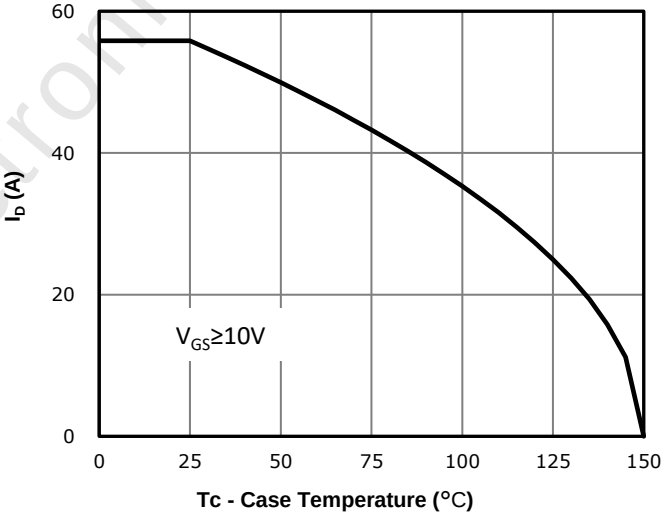


Fig 11: Safe Operating Area

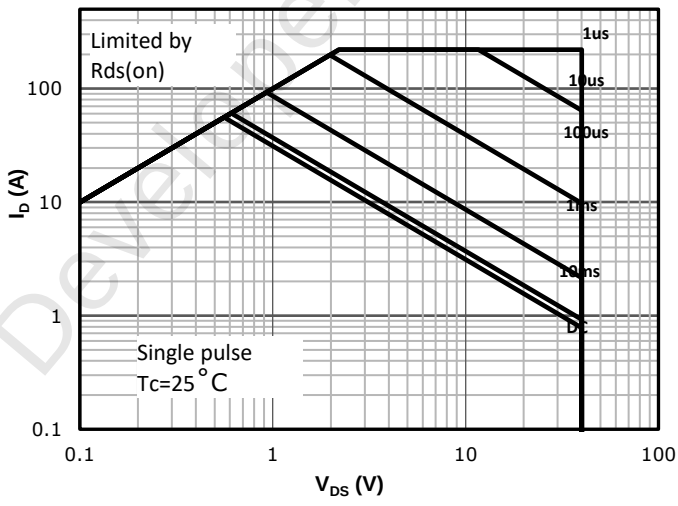
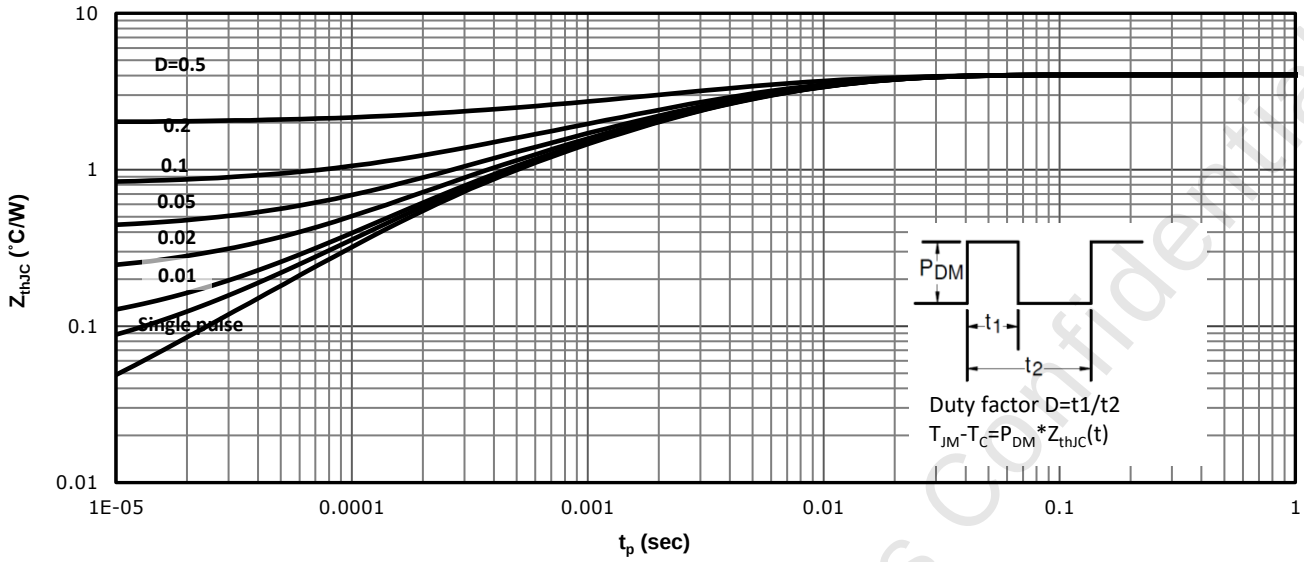
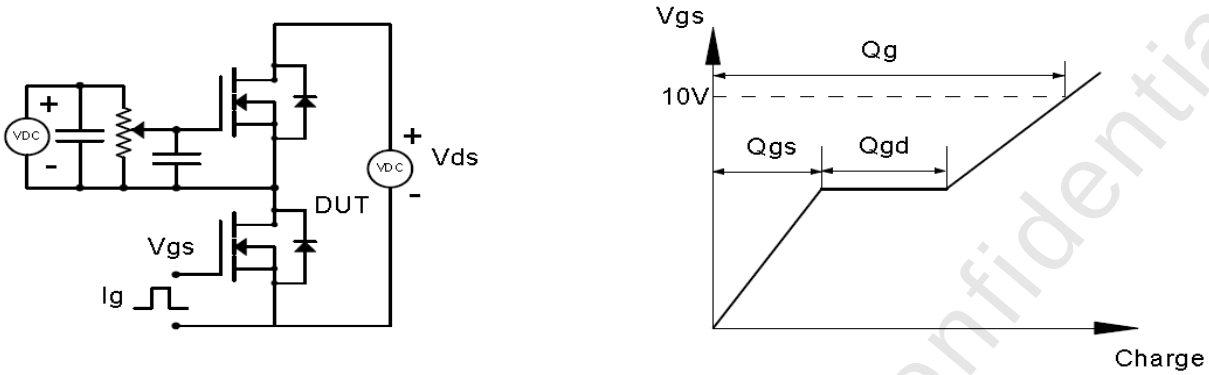


Fig 12: Max. Transient Thermal Impedance

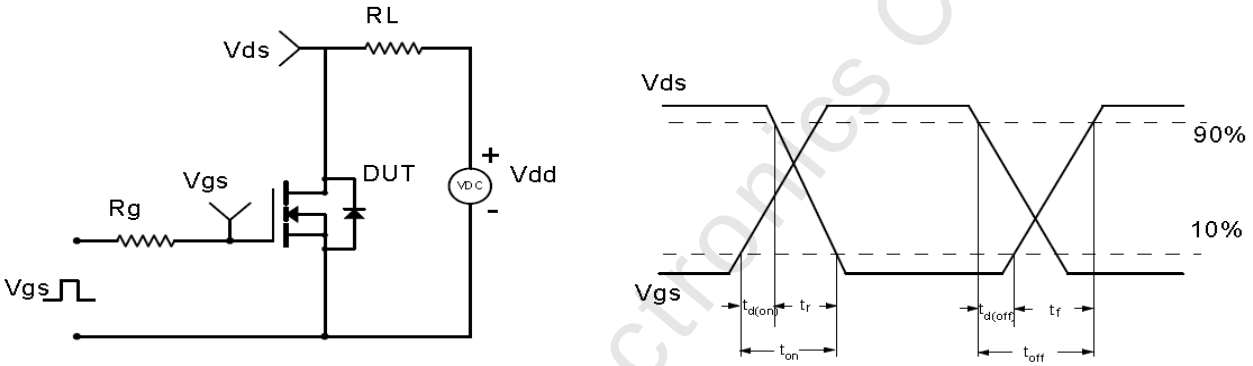


Test Circuit & Waveform

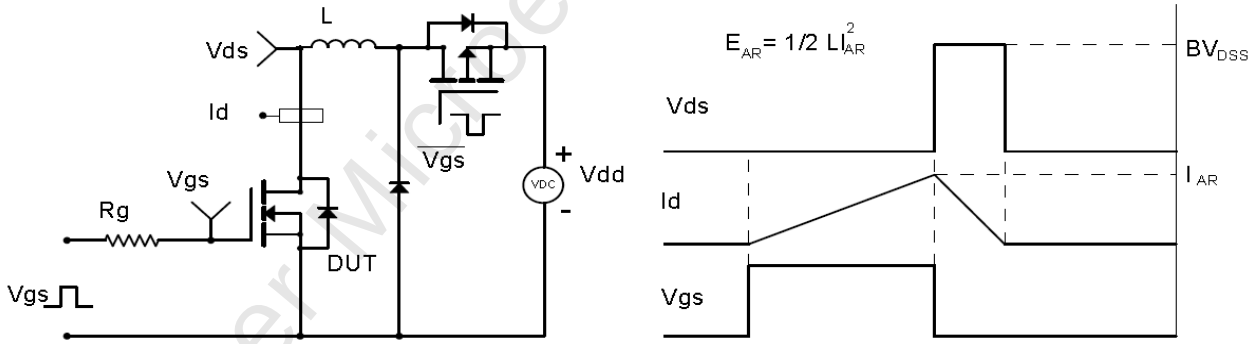
Gate Charge Test Circuit & Waveform



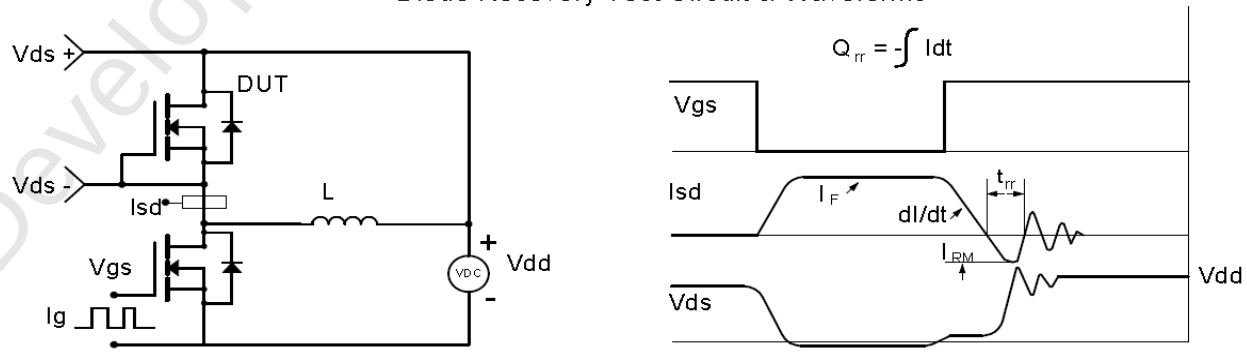
Resistive Switching Test Circuit & Waveforms



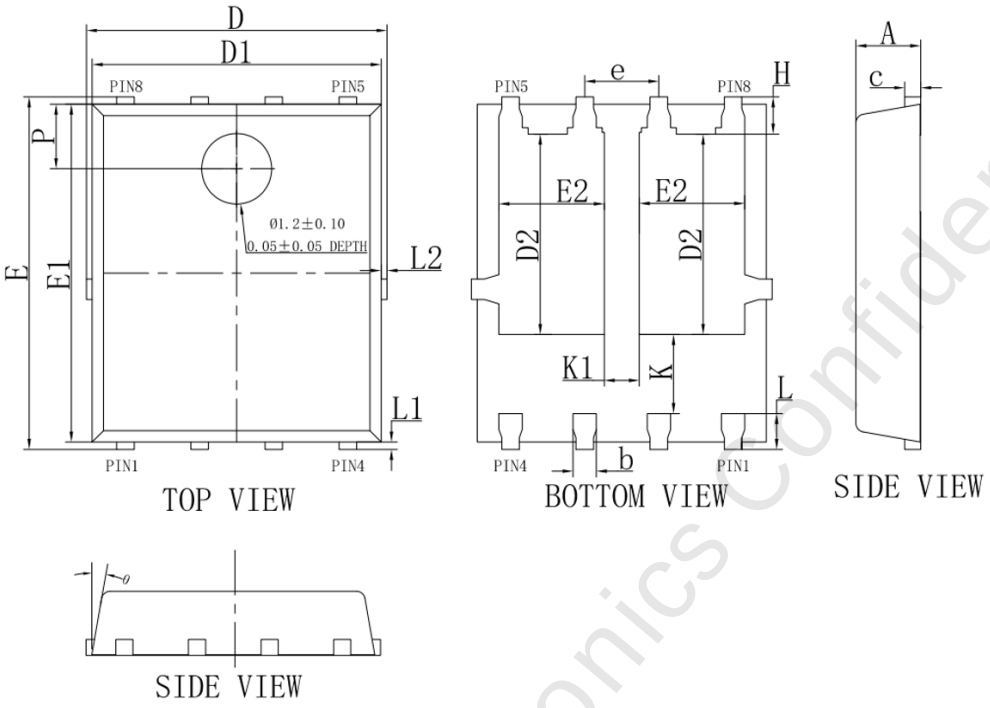
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

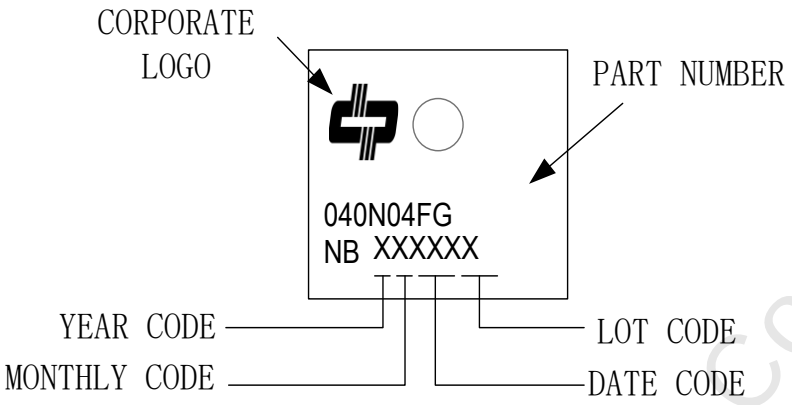


Package Outline: DFN5x6-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.00	1.20	0.039	0.047
D	-	5.10	-	0.201
D1	4.90	5.00	0.193	0.197
D2	3.31	3.51	0.130	0.138
E	5.90	6.10	0.232	0.240
E1	5.70	5.80	0.224	0.228
E2	1.71	1.91	0.067	0.075
H	0.51	0.71	0.020	0.028
b	0.35	0.45	0.014	0.018
c	0.21	0.34	0.008	0.013
e	1.17	1.37	0.046	0.054
K	1.25	1.45	0.049	0.057
K1	0.50	0.70	0.020	0.028
L2	0.51	0.71	0.020	0.028
L1	0.06	0.20	0.002	0.008
L2	-	0.15	-	0.006
P	1.00	1.20	0.039	0.047
θ	8°	12°	-	-

Part Marking Information



Revision History

Revison	Major changes
1.0	Release for formal version

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