40V, 0.6A 1.1MHZ Synchronous Buck Converter

FEATURES

- Up to 95% Efficiency
- Input Voltage Range: 4V to 40V
- Output Voltage Range: 0.8V to 20V
- Continuous Output Current: 0.6A
- CCM Switching Frequency: 1.1MHz
- Reference Voltage: 0.8V ±2% @25℃
- Maximum Duty Cycle: 95%
- Integrated MOSFETs: 450mΩ and 240mΩ
- Low Quiescent Current: 90μA
- Low Shutdown Current: 2.5μA
- Optional Operation Modes at Light-Load Condition:
  - DP31240B: Power Save Mode (PFM)
  - DP31240FB:Continuous Current Mode(FPWM)
- Over Current Protection
- Short Protection with Hiccup-Mode
- Internal Soft Startup
- Thermal Shutdown Protection

DESCRIPTIONS

The DP31240B/FB is a low EMI signature, synchronous, step-down, Current mode converter with internal power MOSFETs. It offers a very compact solution to provide 0.6A continuous current over a wide input supply range, with excellent load and line regulation. DP31240B/FB achieves low EMI signature with well controlled switching edges. Fault condition protection includes programmable -output over-voltage protection, and thermal shutdown. package.

DCM/CCM mode operation provides very low output ripple voltage for noise sensitive applications. Switching frequency is internally. set at 600KHZ, allowing the use of small surface mount inductors and capacitors. Low output voltages are easily supported with the 0.8V feedback reference voltage.

The DP31240B/FB requires a minimal number of readily available, external components and is available in a small package.

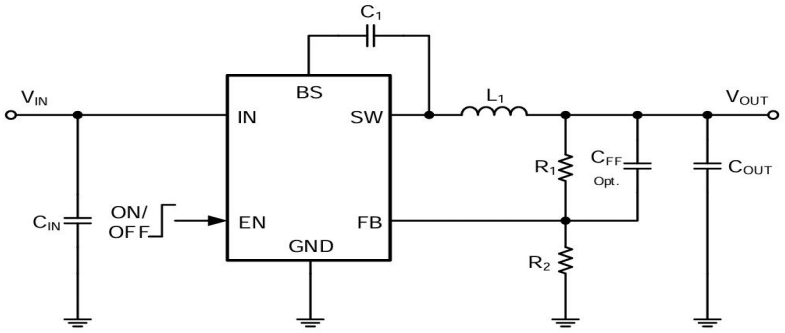
APPLICATIONS

- Electric Tool
- White Goods, Small Household Appliances
- Audio, WIFI
- 12V, 24V Distributed Main Power Supply

ORDERING INFORMATION

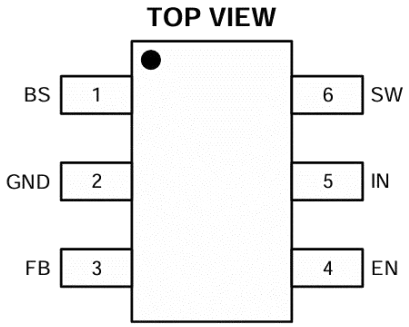
Part Number	Description	Moisture sensitivity level
SOT23-6	Pb free in T&R, 3000 Pcs/Reel	MSL=3

TYPICAL APPLICATION CIRCUIT



PRODUCT DESCRIPTION

➢ Pin Arrangement



SOT23-6

➢ Pin Configuration

SOT23-6	Pin Name	Description
1	BS	Supply input for the high-side NFET gate drive circuit. Connect a 0.1μF capacitor between VBST and SW pins.
2	GND	Ground Pin
3	FB	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
4	EN	Chip Enable Pin. Drive EN above 1.4V to turn on the part. Drive EN below 0.4V to turn it off.
5	IN	Power supply voltage input.
6	SW	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.

➢ Marking Information

DP31240 for product name:

YYY refers to the following table description, represents different packaging and special functions

XXXX The first X represents the last year,2020 is 0;The second X represents the month,inA-L 12 letters;The third and fourth X on behalf of the date,01-31said;

Marking	Model	Description
31240B	DP31240BST	DP31240BST Buck，4V~40V，0.6A，1.1MHZ，VFB 0.8V，**PFM**，SOT23-6
31240FB	DP31240FBST	DP31240FBST Buck，4V~40V，0.6A，1.1MHZ，VFB 0.8V，**FPWM**，SOT23-6

➢ Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)(1)

PARAMETER	Min	Max	Unit
VIN Voltage	-0.3	45	V
EN Voltage	-0.3	45	V
SW Voltage(DC)	-0.3	45	V
SW Voltage(AC less than 10ns while Switching)	-3	45	V
FB Voltage	-0.3	6	V
BS Voltage(vs SW)	-0.3	6	V
Operating junction temperature,TJ	-40	150	℃
Storage temperature, Tstg	-65	150	℃
Lead Temperature（Soldering，10sec.)	-	260	℃

Note:(1)Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute – maximum – rated conditions for extended periods may affect device reliability.

（2）All voltage values are with respect to network ground terminal

➢ Recommended Operating Conditions

PARAMETER	Min	Max	Unit
VIN Voltage(V_{IN})	4	40	V
Output current(I_{OUT})	0	0.6	A
TJ	-40	125	℃

Note : (1)All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

➢ ESD Ratings

PARAMETER	Description	Value	Unit
HBM	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
CDM	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

Note : (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

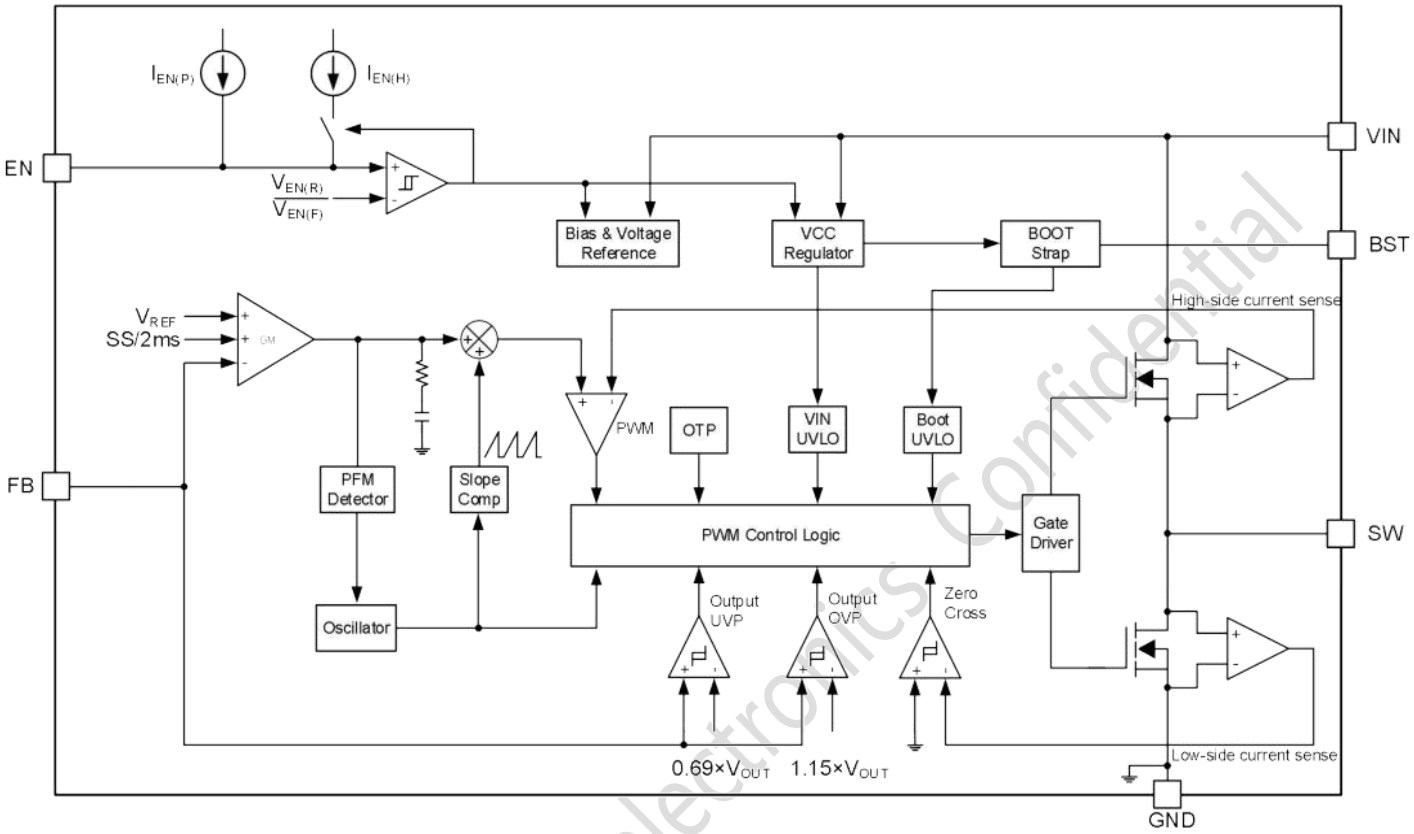
➢ Thermal Information

THERMAL METRIC	Description	SOT23-6	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)(2)	121.6	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.1	℃/W
$R_{\theta JB}$	Junction-to-board(Bottom) thermal resistance	45.5	℃/W
ψ_{JT}	Junction-to-top characterization parameter	22.3	℃/W
ψ_{JB}	Junction-to-board characterization parameter	46	℃/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Typical at Vin=12V,TJ=25°C, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}		4		40	V
VIN Quiescent Current	I_Q	No-switching, V_{EN}=12V, V_{FB}=V_{REF}*105%, Iout=0A		90		uA
Shutdown Current	I_{SHDN}	V_{EN}=0V		2.5		uA
VIN UVLO Rising Threshold	$V_{UVLO(R)}$	V_{IN} Rsing		3.8		V
VIN UVLO Falling Threshold	$V_{UVLO(F)}$	V_{IN} Falling		3.5		V
VIN UVLO Hysteresis	$V_{UVLO(HYS)}$			0.3		V
FB Voltage	V_{FB}	T_J=25℃	0.792	0.8	0.808	V
FB Leakage Current	$I_{FB(LkG)}$	T_J=25℃	-100	10	100	nA
Switching Frequency	Fsw	V_{OUT}=1.2V, Operation CCM		1.1		MHZ
Max duty cycle	Dmax				95	%
Mini on Pulse Width	$T_{ON(MIN)}$			70		ns
High-Side Switch Current Limit	$I_{HS(OC)}$	V_{IN}= 12V, V_{FB}=90%		1.3		A
Low-Side Switch Current Limit	$I_{LS(OC)}$	V_{IN}= 12V, V_{FB}=90%		0.8		A
Low-Side Switch Current Limit_N	$I_{LS\_N(OC)}$	FCCM Olny		0.4		A
High-Side MOS ON-Resistance	$R_{DSON(HS)}$	Isw=100mA		450		mΩ
Low-Side MOS ON-Resistance	$R_{DSON(LS)}$	Isw=100mA		250		mΩ
VOUT OVP Rising Threshold	$V_{OVP(R)}$	VOUT Rising		115		%
VOUT OVP Falling Threshold	$V_{OVP(F)}$	VOUT Falling		111		%
VOUT UVP Rising Threshold	$V_{UVP(R)}$	VOUT Rising		72.5		%
VOUT UVP Falling Threshold	$V_{UVP(F)}$	VOUT Falling		69		%
EN Rising Threshold	$V_{EN(R)}$	EN Rising	1.1	1.23	1.36	V
EN Falling Threshold	$V_{EN(F)}$	EN Falling	0.95	1.1	0.22	V
EN Hysteresis	$V_{EN(HYS)}$			0.12		V
Soft Start	Tss	10%*Vout to 90%*Vout		2		ms
Over-Temperature Protection	T_{SD}			160		℃
Over-Temperature Protection hysteresis	$\triangle T_{SD}$			30		℃

TYPICAL CHARACTERISTICS

Test Condition：TA = 25℃，VIN=12V，Vout=5V，unless otherwise noted.

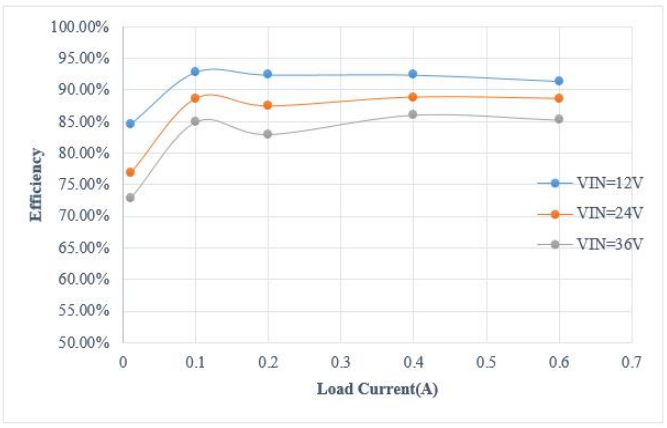


Figure1 5V Output Efficiency

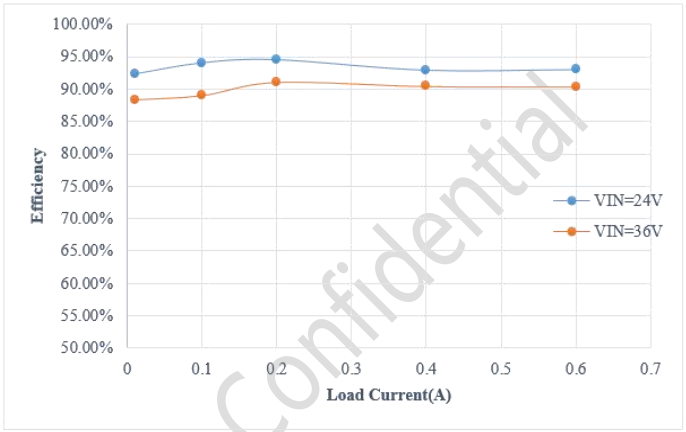


Figure2 12V Output Efficiency

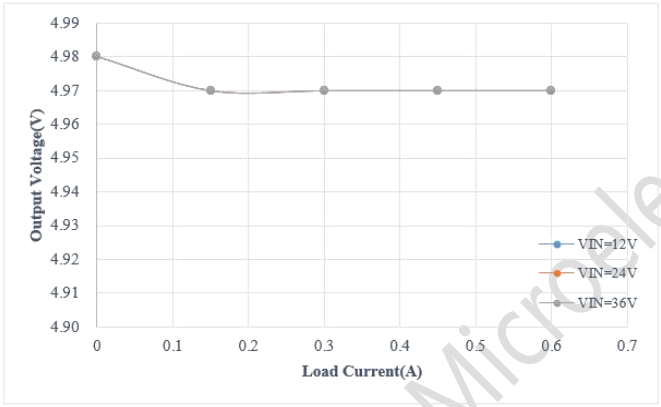


Figure3 5V Output Load Regulation

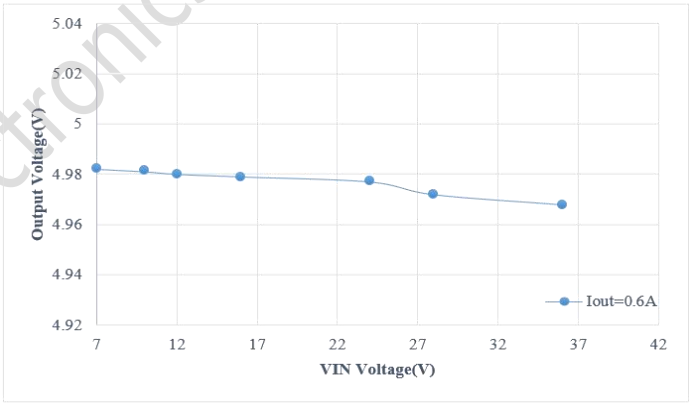
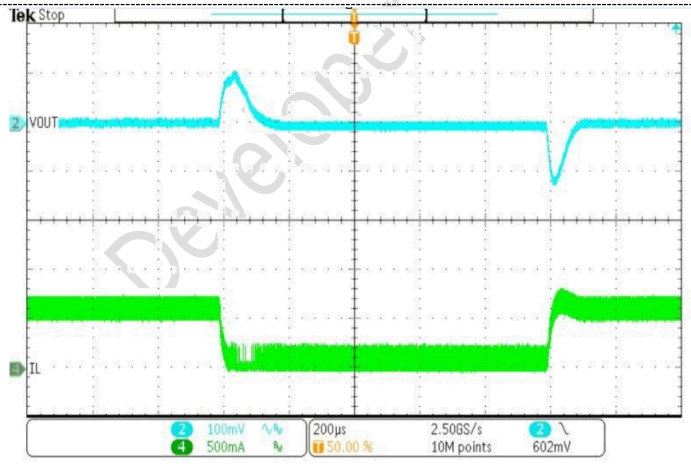
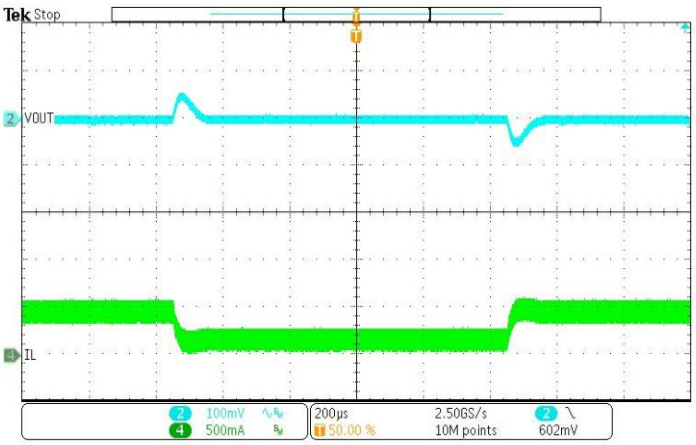


Figure4 Line Regulation Iout=0.6A



Load Step 0.1 to 0.6A, 1A/us Slew rate

Figure5 Load Transient



Load Step 0.15 to 0.5A, 1A/us Slew rate

Figure6 Load Transient

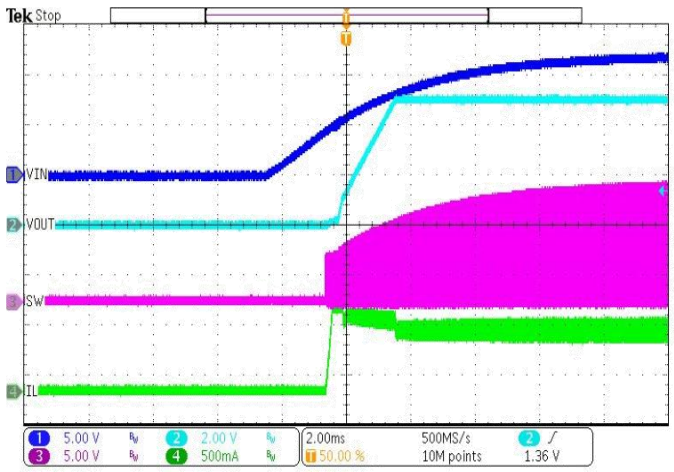


Figure7 VIN StartUp with Load

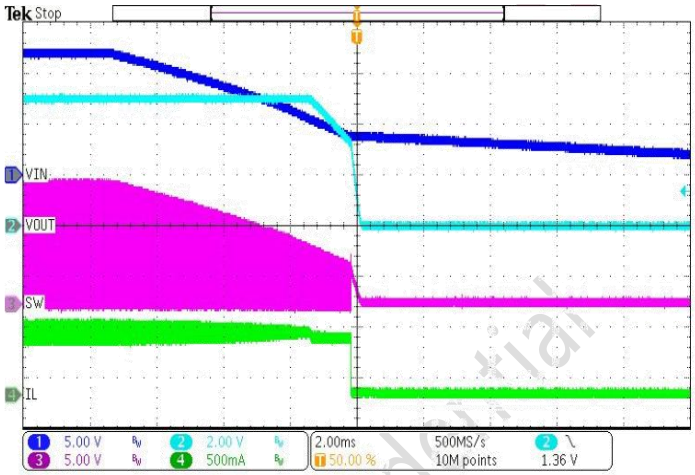


Figure8 ShutDown with Load

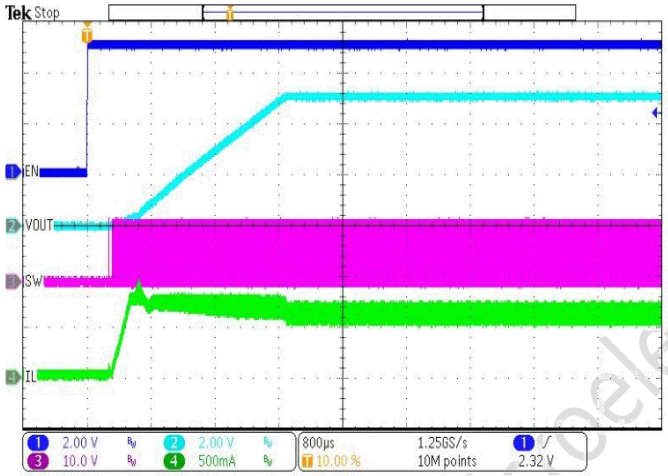


Figure9 EN StartUp with Load

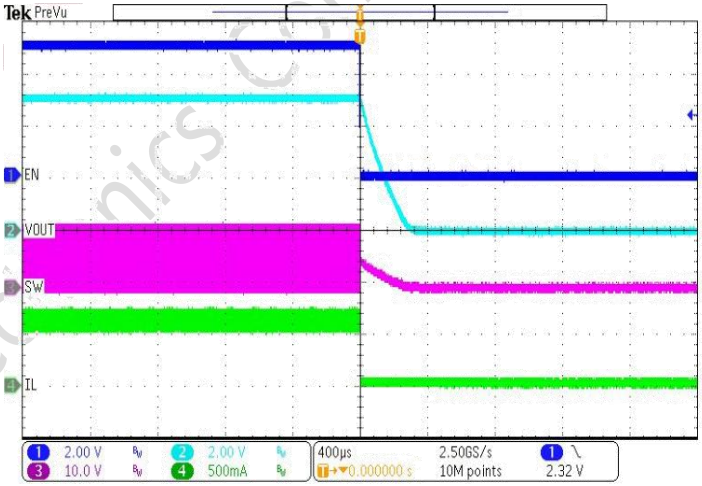


Figure10 EN ShutDown with Load

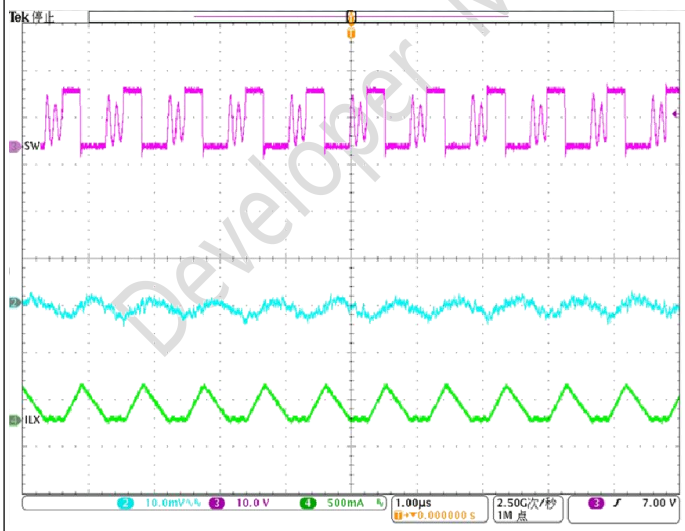


Figure11 DCM with Iout=0.1A

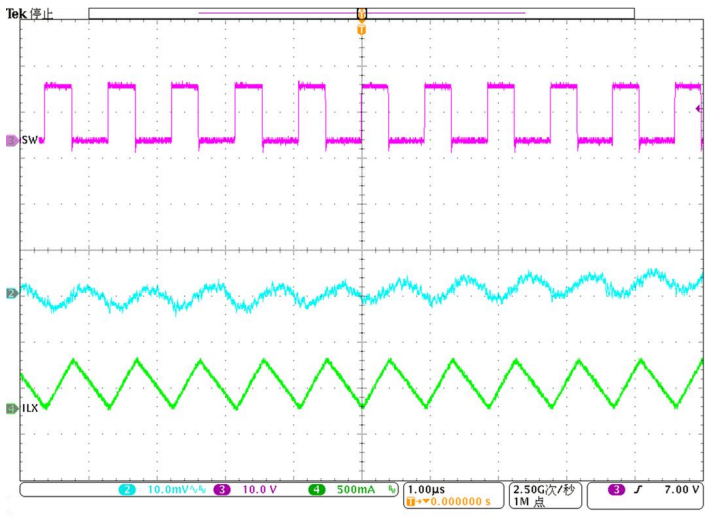


Figure12 CCM with Iout=0.3A

FUNCTIONS DESCRIPTION

- **Feature Description**

The DP31240B/FB is a Current mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 1.5MHz operating frequency to ensure a compact, high efficiency design with excellent DC performance.

- **Thermal Shutdown**

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160 ° C typically. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

- **Soft Start**

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.8V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally max to 2ms.

- **UNDER-VOLTAGE LOCKOUT (UVLO)**

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

- **OUTPUT Over Voltage Protection(OVP)**

The DP31240B/FB integrates output overvoltage protection function, which can reduce the possible output voltage overshoot in case of chip failure or sudden load reduction, and avoid damage to downstream electrical equipment. When the output exceeds VOVP (R), the VOUT OVP comparator output is set to high, and the integrated high and low side MOSFETs will be turned off to avoid further increase in output. When the output is below VOVP (F), the chip will resume normal operation. The output overvoltage protection function is a non latch function.

- **REVERSE CURRENT PROTECTION(DP31240FB Olny)**

The DP31240FB operates in FPWM mode under light load conditions, allowing low side MOSFETs to pass reverse current. In FPWM mode, if the output terminal is accidentally connected to an external power source, the chip may operate in reverse boost mode, generating high reverse current and damaging the chip. DP31240FB Integrates a low side MOSFET current detection circuit internally. When the reverse current of the low side MOSFET is detected to be greater than the reverse current limit threshold Is (Noc), the low side MOSFET is immediately turned off, and then the high side MOSFET is turned on to discharge the energy of the output inductor. This function can limit the reverse current to remain above the reverse current limit threshold, thereby protecting the low side MOSFET. In addition, the reverse current limiting function does not take effect within the minimum turn off time

- **Low Dropout Mode**

In CCM operation, the switching frequency is fixed, and the minimum and maximum duty cycle values **Dmin** and **Dmax** of the converter are respectively affected by the shortest conduction time **ton (min)** and **toff (min).**

$$D_{min} = t_{ON(min)} \times f_{SW} \quad (1)$$

$$D_{max} = 1 - t_{OFF(min)} \times f_{SW} \quad (2)$$

Given the output voltage, the maximum operational input voltage is:

$$V_{IN(max)} = \frac{V_{OUT}}{D_{min}} \quad (3)$$

Given the output voltage, the minimum operable input voltage is:

$$V_{IN(min)} = \frac{V_{OUT}}{D_{max}} \quad (4)$$

Considering the voltage drop in the power circuit, the actual maximum/minimum operable input voltage will be greater/less than the calculated value mentioned above.

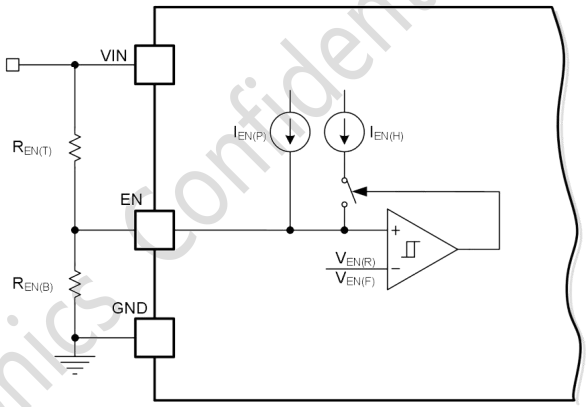
When the input voltage approaches the output voltage, in order to maintain the maximum output voltage as much as possible, the chip will reduce the operating switching frequency. Due to the fixed toFF (min), the conduction time of the high side MOSFET will be extended up to a maximum of 3.5us (typical value)

- **EN enable control**

DP31240X provides an external enable control pin (EN) to enable or disable chip operation. When the EN pin voltage is higher than the EN rising voltage ($V_{EN(R)}$) and the IN voltage is higher than the VIN undervoltage lock threshold ($V_{UVLO(R)}$), the chip enables normal operation.

If the EN pin voltage is pulled below the threshold voltage ($V_{EN(F)}$), the chip stops switching and enters shutdown mode. Even if the VIN voltage is higher than the VIN undervoltage lock threshold ($V_{UVLO(R)}$), the chip is disabled and the switching action stops. In shutdown mode, the input current of the chip decreases to the lowest shutdown current (typical value is 2.5 μ A)

The EN pin has an internal pull-up current source, allowing users to keep the EN pin suspended to enable the chip. In addition, according to practical application needs, the EN pin can be connected to an external logic control interface to achieve chip control. The voltage of the EN pin shall not exceed VIN+0.3V. When VIN is 0V, it is not recommended to apply EN voltage.



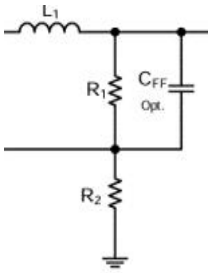
APPLICATION INFORMATION

The output stage of synchronous buck converter is mainly composed of inductor and capacitors. By switching the internally integrated power MOSFET, the energy is stored and transferred to the load, and the second-order LC filter is formed to smooth the switching node voltage so that the stable output DC voltage is obtained.

- **Setting Output Voltage**

The output voltage is set by FB voltage, which is divided by resistor (R1 & R2) from output node to Ground. That resistor with 1% or higher accuracy is preferred. The output voltage value is set by equation as below.

$V_{OUT}=V_{FB} \times ((R1+R2)/R2)$



Vref is the internal reference voltage of DP31240B/FB, 0.8V.

Table1 Recommend Component Selection Table

VOUT (V)	R1 (kΩ)	R2 (kΩ)	BS (uF)	L1 (uH)	CIN (uF)	COUT (uF)	CFF(pF) Opt.
1.05	6.25	20	0.1	2.2	22	44	Opt.
3.3	31.6	10	0.1	4.7	22	44	Opt.
5	52.3	10	0.1	6.8	22	44	Opt.
9	102	10	0.1	8.2	22	44	Opt.
12	140	10	0.1	10	22	44	Opt.
20	240	10	0.1	22	22	44	Opt.

- **Inductor selection**

An inductor is required to supply constant current to the load while being driven by the switched input voltage. The common value of the inductance is between 2.2uH to 22uH. A larger value inductor will result in less current ripple and lower output voltage ripple. However, the larger value inductor will have larger physical size, higher DC resistance, and/or lower saturation current. A good rule to calculate the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current. At the same time, it is needed to make sure that the peak inductor current is below the inductor saturation current.

The inductance value can be calculated by:

$$L=\frac{V_{OUT}}{f_s \times \Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where VOUT is the output voltage, VIN is the input voltage, fs is the switching frequency, and ΔL is the peak-to-peak inductor ripple current.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency

- **Input capacitors selection**

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the converter. It is recommend to use low ESR capacitors to optimize the performance. Ceramic capacitor is preferred, but tantalum or low-ESR electrolytic capacitors may also meet the requirements. It is better to choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (CIN) absorbs the input switching current, a good ripple current rating is required for the capacitor. The RMS current in the input capacitor can be estimated by:

$$I_{CIN}=I_{load}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at VIN = 2 × VOUT, where:

$$I_{CIN}=\frac{I_{load}}{2}$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current. When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When ceramic capacitors are used, make sure that they have enough capacitance to maintain voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN}=\frac{I_{load}}{f_s\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

CIN is the input capacitance.

- **Output capacitors selection**

The output capacitor (COUT) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended.
Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_s\times C_{OUT}}\right)$$

Where L is the inductor value, RESR is the equivalent series resistance (ESR) value of the output capacitor and COUT is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_s^{\,2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The DP31212S/FS can be optimized for a wide range of capacitance and ESR values.

- **Feed-Forward Capacitor Selector(CFF)**

DP31240B/FB has internal loop compensation, so adding CFF is optional. Specifically, consider whether to add feed-forward capacitors according to the situation.

The use of a feed-forward capacitor (CFF) in the feedback network is to improve the transient response or higher phase margin. To reduce transient ripple, the feed-forward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and cause more ringing. In the other hand, if more phase margin is desired, the feed-forward capacitor value can be decreased to push the cross frequency to lower region.

the value of feed-forward capacitor (CFF) can be calculated with the following equation:

$$Cff\_op=\frac{1}{2\pi\times f_{\_nocff}}\times\sqrt{\frac{1}{R1}\times\left(\frac{1}{R1}+\frac{1}{R2}\right)}$$

Where F_nocff is the cross frequency. the crossing frequency is generally taken as 1/10 to 1/5 of the switching frequency, R1 and R2 are feedback resistors.

- **Bootstrap Capacitor Selection**

Bootstrap Capacitor Selection A 0.1-μF ceramic capacitor must be connected between the VBST to SW pin for proper operation. recommends to use a ceramic capacitor.

- **PCB Layout**

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R1 and R2, should be kept close to FB pin. Vout sense path should stay away from noisy nodes, such as SW & BS signals and preferably through a layer on the other side of shielding layer.

2. The input bypass capacitor C5 and C2 must be placed as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VIN pin to reduce the high frequency injection current.

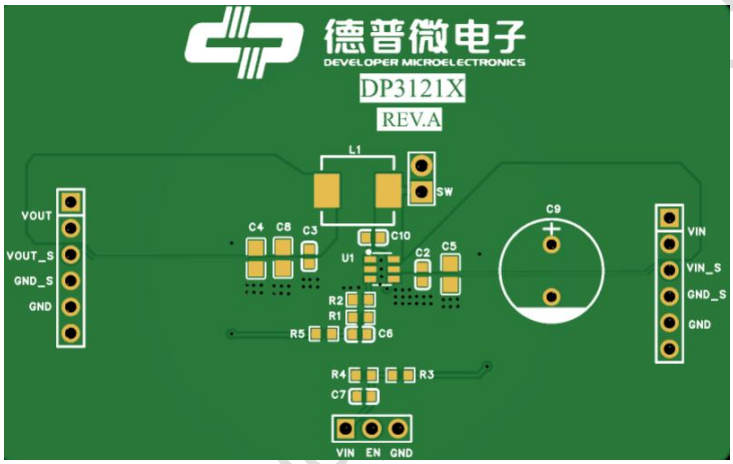
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.

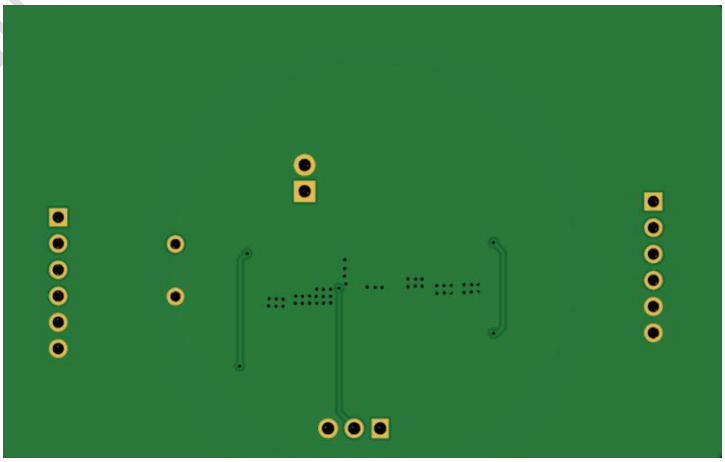
4. The output capacitor, COUT should be placed close to the junction of L1. The L1, and COUT trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.

5. The ground connection for C5, C2 and C8, C4 ,C3 should be as small as possible and connect to system ground plane at only one spot (preferably at the COUT ground point) to minimize injecting noise into system ground plane.

6. Large GND Copper Pour near IC is recommended to minimize the heat of IC.

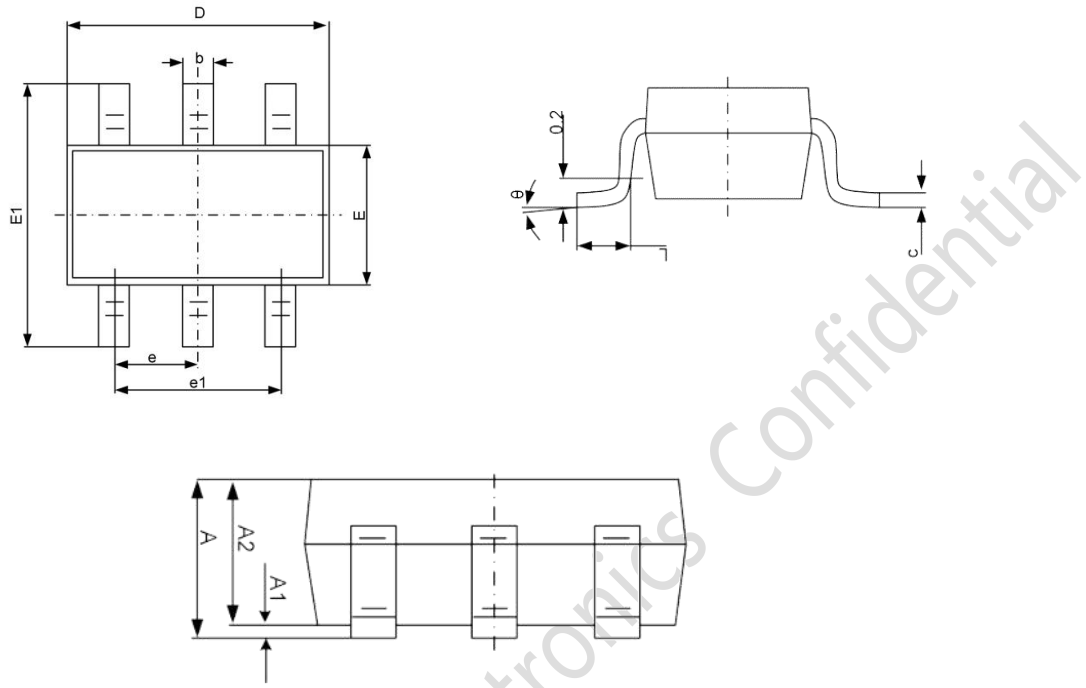
- **Layout Example:**





PACKAGE DIMENSION

SOT23-6



Symbol	Dimensions in Millimeters	
	Min	Max
A	-	1.350
A1	0.000	0.150
A2	1.000	1.200
b	0.300	0.500
c	0.100	0.220
D	2.820	3.020
E	1.500	1.700
E1	2.600	3.000
e	0.950(BSC)	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°

REVISION HISTORY

Editions	Revised Date	Redaction person	Revision content
REV1.0	2025/6/10	PXB	First release

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