LED Common Anode Line Driver IC

1 Overview

DP32030B is a serial decoding line driver chip that is specially designed for LED scan screen. DP32030B can completely replace the original 3-8 decoder (74HC138) circuit of LED module, to greatly simplify the PCB wiring of LED module, and improve the overall image effects of display screen.

2 Characteristics

- Working voltage 2.6V~5.5V
- Support random scan
- Integrate 16-channel power PMOS tube
  - OUT_MAX = 2.5A @ VDD = 5.0V
  - RON=130mΩ@VDD=5.0V&IOUT=1.0A
- Max. power consumption < 600 mW @ VDD = 5.0V
- Integrate shadow elimination self-adaption function, to eliminate the image tail effectively
- The shadow elimination potential can be configured in register, to adapt to a more complex environment
- Improve the cross of display screen due to LED open circuit
- Simplify the PCB wiring of LED module
- Package mode: QSOP24, QFN24
- High ESD level

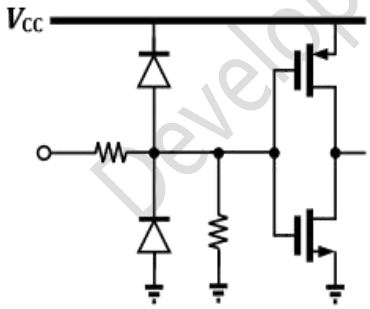
3 Application field

- LED video display with high refresh rate
- Full-color LED display
- High-density small-spacing LED panel display

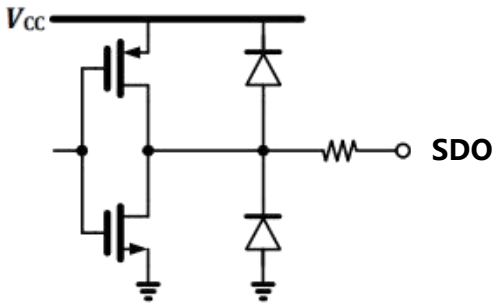
4 Schematic Diagram of Circuit

4.1 Input/output equivalent circuit

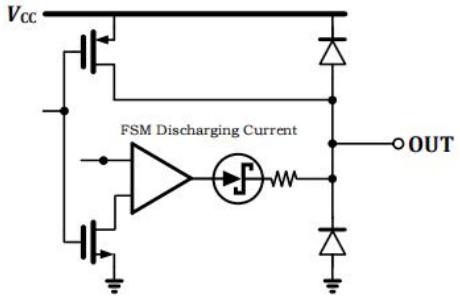
DIN,DCK,RCK input end



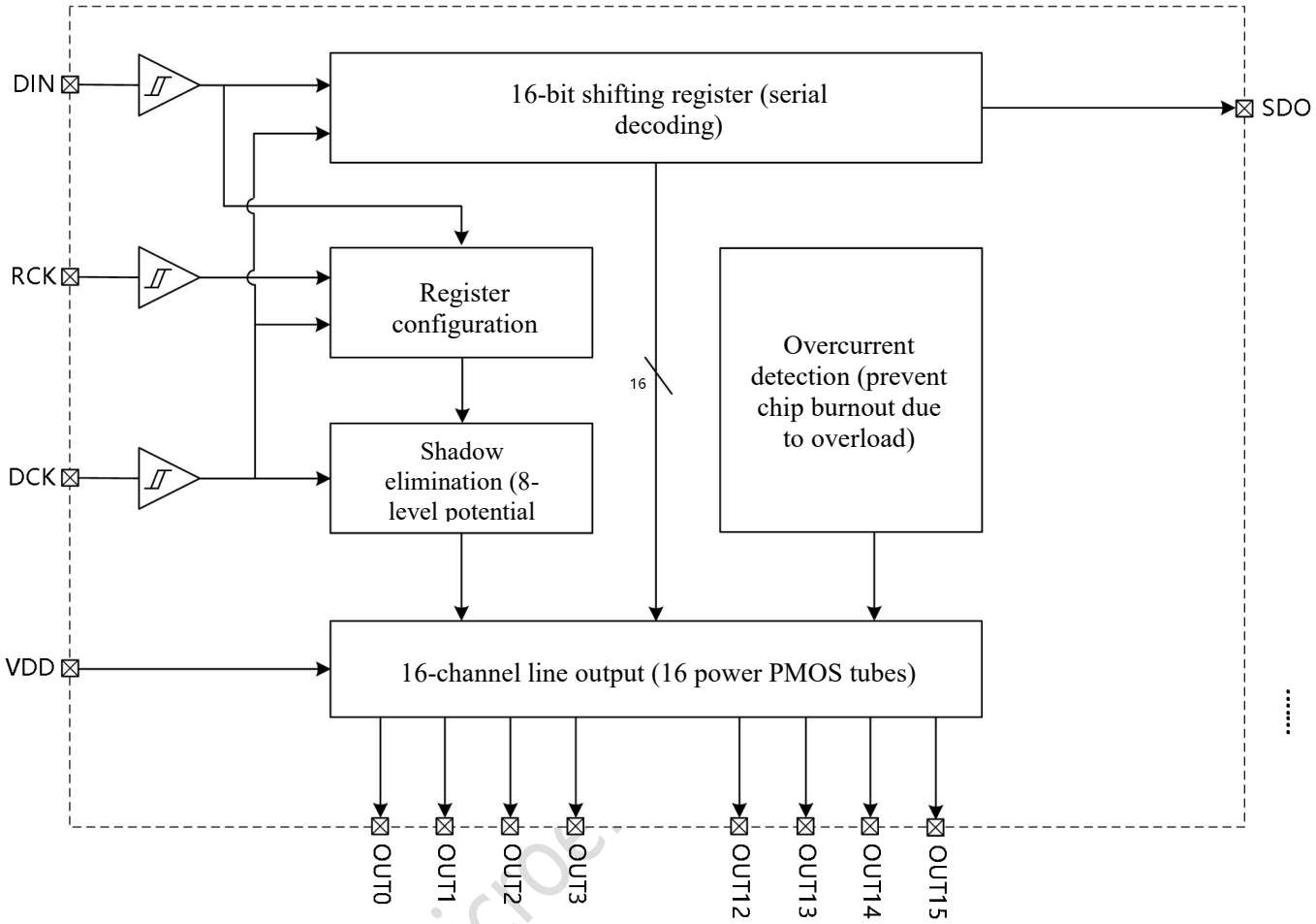
SDO output end



OUT0~7 output end



4.2 Block Diagram of Internal Circuit



Contents

Revision History

Ver.	Revision Date	Revised by	Revision Content
V1.0	2023.09	WM	1. Initial version
V1.1	2023.11	WM	1. Modify shadow elimination voltage level 2. Modify document font
V1.2	2024.05	WM	1. Add QFN package
V1.3	2024.05	WM	1. Modify register configuration
V1.4	2024.06	WM	1. Modify supported scan number
V2.0	2025.03	WM	1. Modif Product mark and DC electrical characteristic

5 Product Introduction

- Pin definition

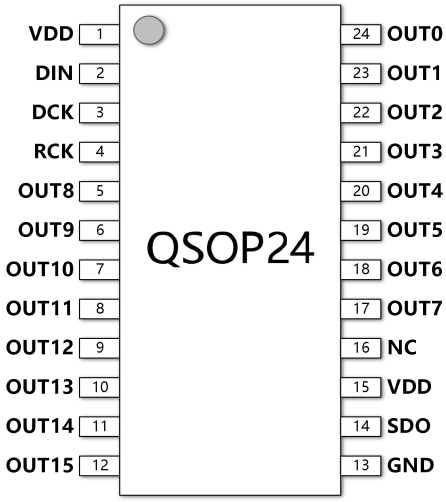


Diagram of QSOP24 Pin Definition

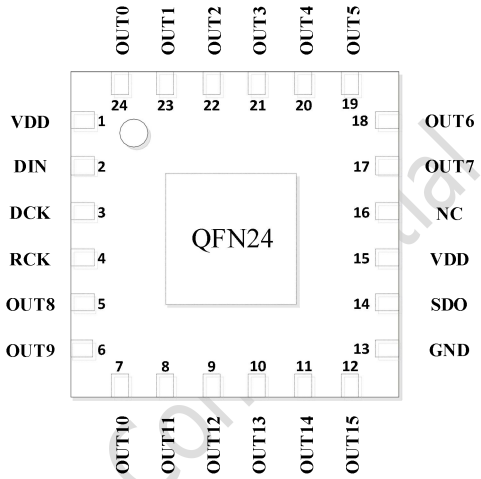


Diagram of QFN24 Pin Definition

- Pin Description

QSOP24 pin number	QFN24 pin number	Pin name	Pin Description
1, 15	1, 15	VDD	Power input
2	2	DIN	Data input
3	3	DCK	Serial signal clock input
4	4	RCK	Blanking register configuration clock input
5~12, 17~24	5~12, 17~24	OUT0~OUT15	OUT output
13	13	GND	Ground
14	14	SDO	Serial data output
16	16	NC	Empty pin

- Product order information

Product name	Package Type	Package mode	Quantity/disc	Humidity sensitivity level
DP32030B	QSOP24	Braid	4000	MSL=3
	QFN24	Braid	5000	

- Product mark

QSOP24

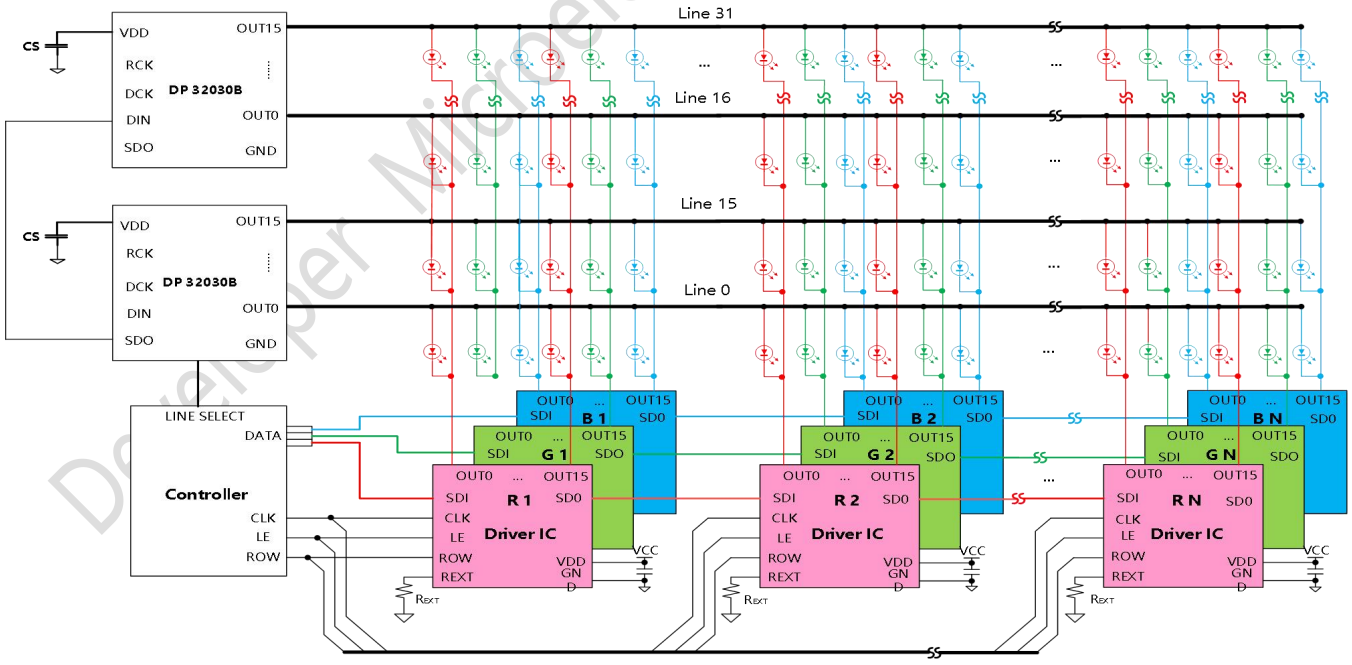
QFN24

DP32030B is product name, XXXXXX means product batch number

6 Suggested application circuit

As LED scan screen is widely applied in indoor display screen for reducing the cost, the capacitor parasitics of LED anode may generate discharge path instantaneously while changing scan and thus causing image tail of display screen; the user can use the DP32030B that supports discharge circuit function by referring to the suggested application circuit of scanning screen in picture below, and set up the constant-current driver chip DP3265S that has built-in pre-charge function, in order to completely eliminate the upper/lower image tail.

As DP32030B is a 16-way output integrated power chip, it is suggested to use the display screen above 16 scans to avoid heat accumulation, and pay attention to the temperature while using it.



Block Diagram of 32-scan Application of LED Display Screen

7 Parameter Table

7.1 Max. limit parameters

Item	Symbol	Rated value	Unit
Power voltage	VCC	0~6.0	V
Input voltage (all pins)	VIN	-0.4~VDD+0.4	V
Continuous working current of OUT end	ID	-2.5	A
Instantaneous max. current of OUT end	IOUT_MAX	-3.5	A
Power loss	PD	<600	mW
Package thermal resistance	Rth(j-a)	80	℃/W
Working temperature	Topr	-40~85	℃
Storage temperature	Tstg	-40~150	℃
HBM human body mode	VESD	≥8	KV

- All voltage values are acquired by taking chip ground end (GND) as reference point, the test temperature of max. limit parameter is 25℃.
- The component may have permanent damage when the actual conditions exceed the specified value; the component reliability can be weakened when the actual conditions are below the max. value and they have long-term functioning. The values above are some specified values. The product does not support function operation under unspecified conditions.
- The peak welding temperature of SMT product should not exceed 260℃, the temperature curve is set by manufacturer according to J-STD-020 standard, by referring to the factory realities and suggestions of solder paste manufacturer.

7.2 Recommended working scope

Item	Symbol	Test conditions	Min Value	Typical Value	Max Value	Unit
Power voltage	VCC	—	2.6	5.0	5.5	V
Output end voltage (DOUT)	VDOUT	—	0.7	—	VDD	V
Output end current (DOUT)	IOH	VOH =VDD -0.5V	—	-16	—	mA
	IOL	VOL =0.5V	—	20	—	
Input voltage (DIN,DCK,RCK)	VIH	VDD=3.3V~5.5V	0.7 VDD	—	VDD	V
	VIL		0	—	0.3VDD	

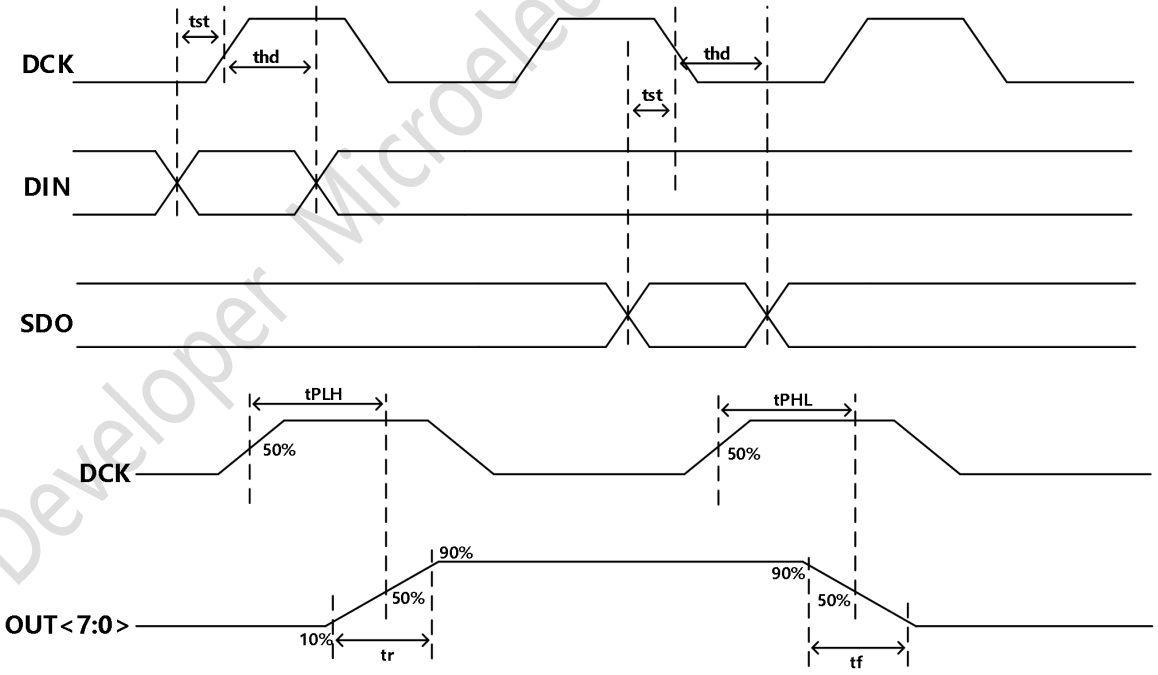
7.3 DC electrical characteristic (VDD=5.0V)

Item		Symbol	Test conditions	Min Value	Typical Value	Max Value	Unit
Logic power voltage		VDD	—	2.6	5.0	5.5	V
Power end current		IDD_OFF	Set all OUT as low	—	100	—	uA
Gate opening voltage		VGS(th)	VDS=VGS,ID=250uA	—	-0.7	-0.9	V
Source - drain electrode conduction resistance		RDS(on)[1:7]	VGS=-5.0V, IOUT=-1.0A	—	130	150	mΩ
Input voltage	High level	VIH	Logic potential	0.7 VDD	—	VDD	V
	Low level	VIL		0	—	0.3 VDD	

7.4 Dynamic characteristics (unless otherwise specified, VDD=3.5V~5V, Ta=25℃)

Item	Symbol	Test conditions	Min Value	Typical Value	Max Value	Unit
Output rise delay	t_{PLH}	VDD=5.0V CL=12pF	-	50	-	ns
Output drop delay	t_{pHL}		-	100	-	ns
Output rising edge	t_r		-	60	-	ns
Output drop edge	t_f		-	400	-	ns
Set-up time	t_{st}		60	-	-	ns
Hold time	t_{hd}		60	-	-	ns

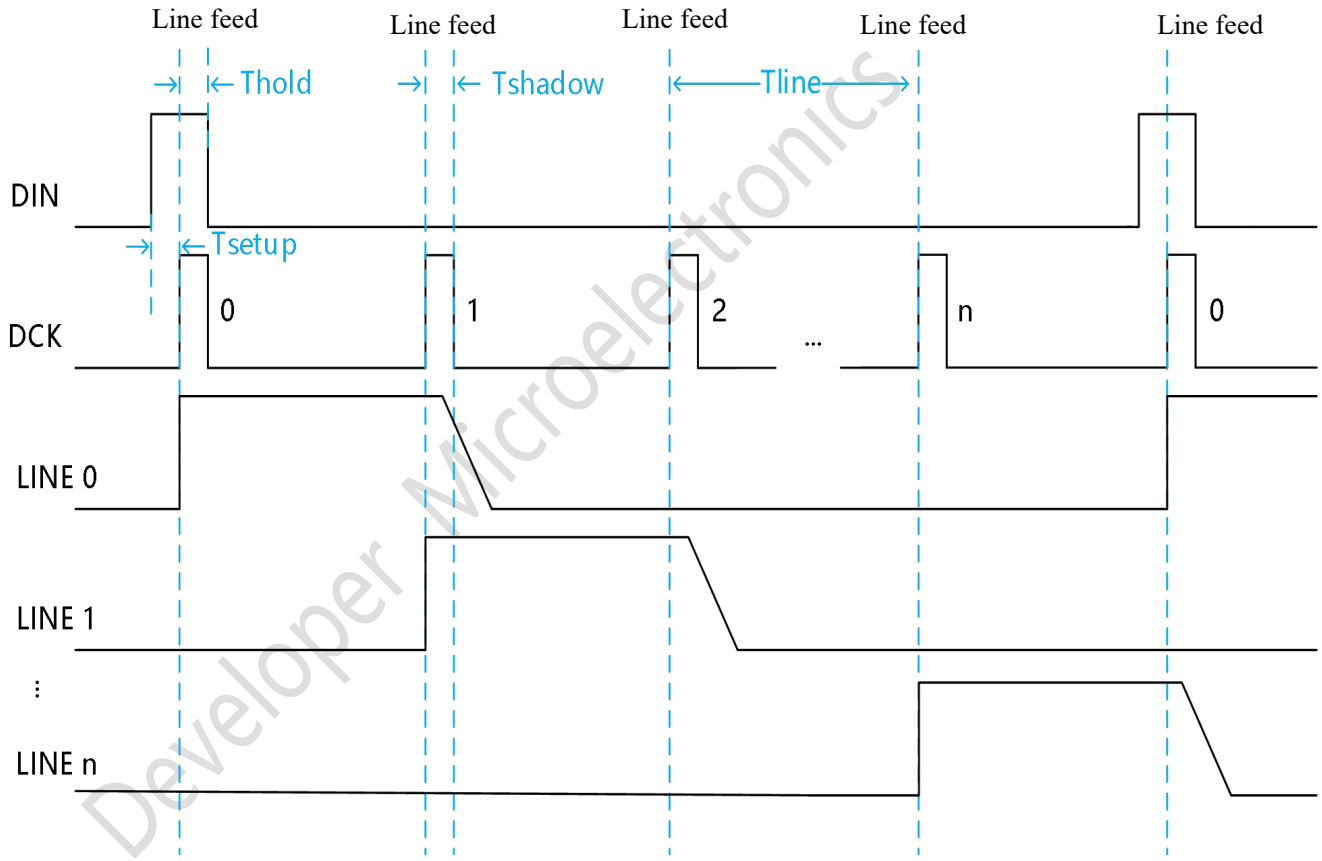
8 Timing waveform diagram



9 Line feed control and shadow elimination time

DP32030B is the drive for serial decoding line of common anode display screen, and 1 DCK is sent during each line feed, channel output is valid; the time from input data DIN to output data DOUT is 16 DCK rising edge intervals.

Symbol	Description	Min Value	Max Value
Tshadow	Shadow elimination time equals to DCK high level width	500ns	-
Tsetup	Setup time	60ns	-
Thold	Hold time	60ns	-

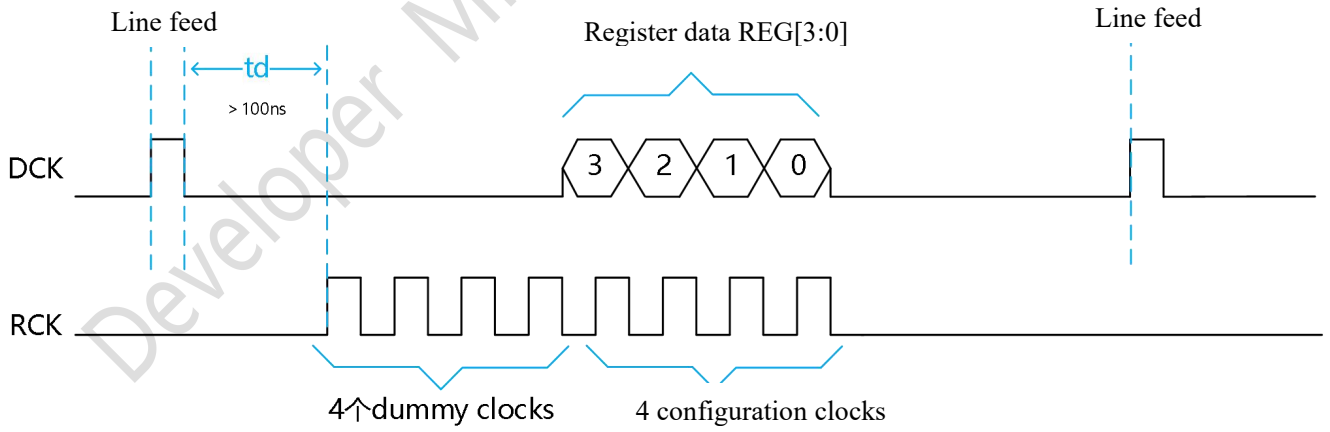


9.1 Register configuration

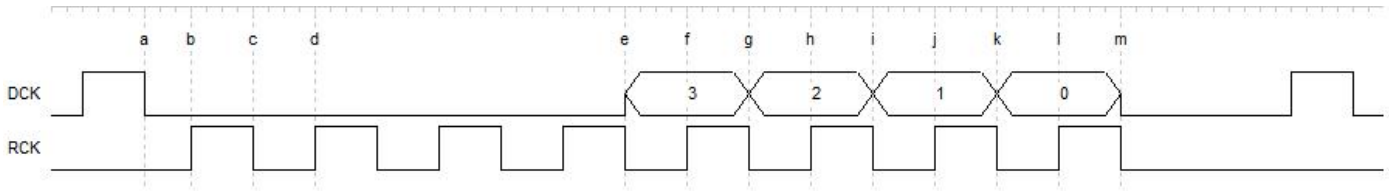
DP32030B built-in 4bit register:

BIT	Name	Default value	Description		
3	VR_UP[2]	1’ b1	Refer to the top digit of potential configuration register VR_UP[2:0] for the pull-up shadow elimination circuit		
2	reserved	1’ b0	/		
1:0	VR_UP[1:0]	2’ b10	The reference potential of pull-up shadow elimination circuit can be configured as (Vdd=5V) by referring to register VR_UP[2:0]		
			0000:Vdd*11/20 =1.75V 0001:Vdd*12/20 =2.0V 0010:Vdd*13/20 =2.25V 0011:Vdd*15/20 =2.5V	1000:Vdd*11/20 =2.75V 1001:Vdd*12/20 =3.0V 1010:Vdd*13/20 =3.25V 1011:Vdd*15/20 =3.5V	Default value 3.25V Correspond to data pins DIN corresponds to Signal C of 3-8 coding DCK corresponds to Signal A of 3-8 coding RCK corresponds to Signal B of 3-8 coding

Configuration method of register: As for 8 clocks (4 dummy clocks+ 4 register configuration clocks) sent by RCK, the register data are sent by DCK during 4 clocks period configured by register.



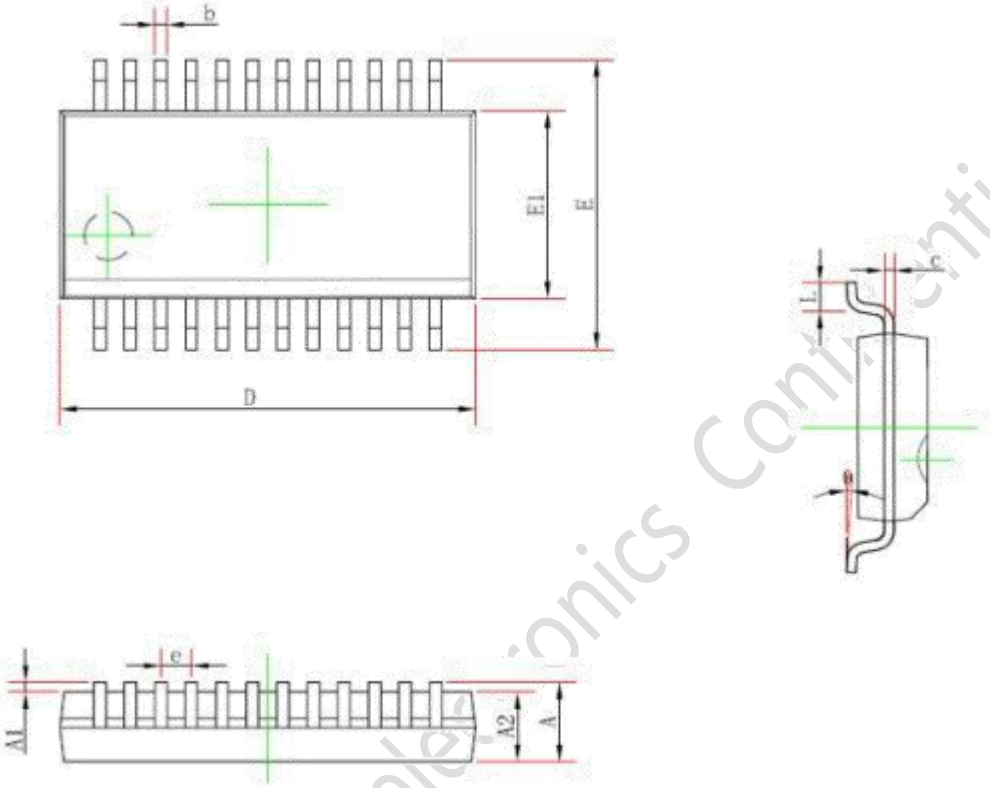
Temporal constraint:



1. ta~tb:>100ns
2. tb~tc(or tc~td):≥60ns (RCK min. pulse width)
3. te~tf(or tg~th or ti~tj or tk~tl)：≥60ns (setup time of register configuration data)
4. tf~tg(or th~ti or tj~tk or tl~tm)：≥60ns (hold time of register configuration data)

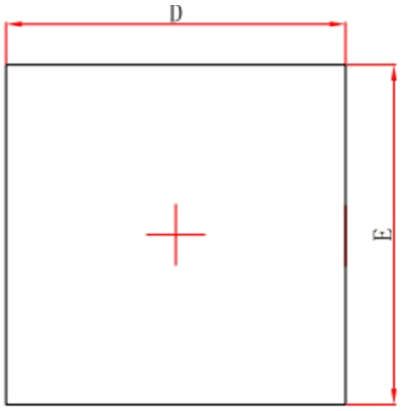
10 Package Information

- QSOP24 plastic package specification diagram

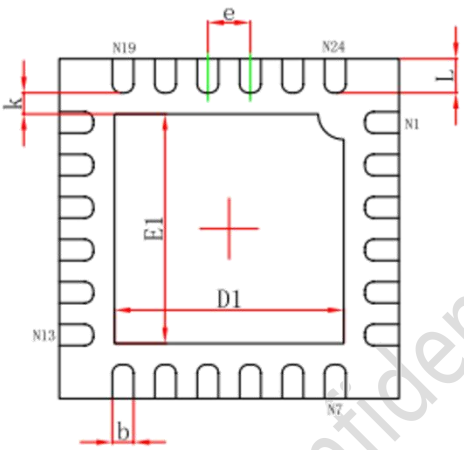


	mm	
	Min	Max
A	—	1.95
A1	0.05	0.35
A2	1.05	—
b	0.1	0.4
c	0.05	0.254
D	8.2	9.2
E1	3.6	4.2
E	5.6	6.5
e	0.635TYP	
L	0.3	1.5
θ	0°	10°

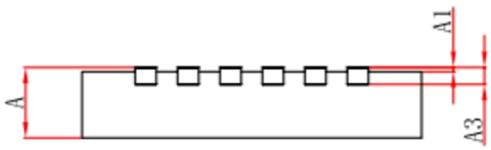
- QFN24 plastic package specification diagram



Top View



Bottom View



Side View

	mm	
	Min	Max
A	0.70	0.80
A1	0.000	0.05
A3	0.203REF	
D	4.00BSC	
E	4.00BSC	
D1	2.625	2.675
E1	2.625	2.675
k	0.275REF	
b	0.18	0.30
e	0.50BSC	
L	0.35	0.45

11 Official Announcement

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